User Guide

SC5-FESTIVAL • CompactPCI® Serial CPU Card

Intel® Mobile Workstation Processor XEON® E3 v6 Family & 7th Generation Intel® Core™ Processor (Kaby Lake)

Document No. 8548 • 8 December 2023

Contents

About this Manual

This manual describes the technical aspects of the SC5-FESTIVAL, required for installation and system integration. It is intended for the experienced user only.

Edition History

Ed.	Contents/Changes	Author	Date
1	User Manual SC5-FESTIVAL, english, preliminary edition (formal structure and some content), Text #8548, File: sc5_ug.wpd	gn	2017-06-07
2	Updated Processor Info and local PCI Device Table; updated section “Hardware Monitor NCT7491"	gn	2017-08-01
2.1	Added photos S40-NVME & S80-P6	jj	3 August 2017
2.2	Added photos S80-P6 with M.2 NVMe loaded	jj	21 August 2017
2.3	Added illustrations 1+4 slots backplane resources	jj	23 August 2017
2.4	Added photos S20-NVME	jj	6 October 2017
2.5	Added MTBF	jj	9 October 2017
3.0	Added SCZ-NVM side card photos, added AMT to table 'Feature Summary'	jj	3 November 2017
3.1	Added photos S82-P6	jj	25 July 2018
4	Added Power requirements	gn	2018-08-03
5	Backplane resources - PCIe root port numbers added	jj	9 August 2018
5.1	Mixup fixed regarding memory speed, added links to SCL & S82 mezzanines	jj	25 September 2018
6	Photos showing SC5-FESTIVAL w. S40-NVME mezzanine updated to S40 PCB rev.1	jj	8 October 2018
6.1	Added photos showing SC5-FESTIVAL w. SCL-RHYTHM side card	jj	23 October 2018
7	Corrected title of CompactPCI Serial Backplane Connectors tables	gn	2019-04-03
8	Added Power requirements SC5-440D	gn	2019-08-30
8.1	Added sample custom backplane illustration for optimized PCIe usage	jj	14 October 2019
9	Added CPCI Hot-Plug UEFI Settings, added Coin Cell Error handling	gn	2020-01-13
10	Added tolerable high voltage level on TTL inputs of expansion connectors	gn	2020-01-24
11	Added P01-M12 (8HP mezzanine, photo)	jj	27 January 2020
12	Added mechanical details (mezzanine connector & mounting hole positions)	jj	29 April 2020
13	PCIe Link width configurable via BIOS setup (HSE2 mezzanine connector)	jj	17 July 2020

Ed.	Contents/Changes	Author	Date
14	Corrected wrong pinout of backplane I^2C in section "Local SMB/I^2C Devices"	gn	2020-09-22
15	Updated MTBF value	jj	2020-09-22
16	Option P01 mezzanine w. M12-X Ethernet connectors Connector P-EXP - UART ports renamed zero based, UART pins configurable as GPIO Added photo SC5-FESTIVAL w. clamshell	jj	8 December 2020
17	Clarified role of CMOS RAM section "Replacement of the Battery" Added UEFI/BIOS setup hint in section "Real-Time Clock"	gn	2021-09-14
18	Changed the type of usable coin cell battery from BR2032 to CR2032	gn	2021-11-26
19	Added PCU-P400-UPTEMPO to list of suitable 8HP mezzanine side cards	jj	23 November 2022
20	ACPI & UEFI Versions updated, S48-SSD low profile mezzanine module added, S83-P6 low profile mezzanine module added, SCJ-VEENA side card added	jj	20 September 2023 26 September 2023
21	Added photos SC5-FESTIVAL w. S83-P6 low profile mezzanine 2.5GbE	jj	8 December 2023

Please note: If an EKF product was labelled  with this special sign according to ISO 7010 M002, please contact support@ekf.com for availability of additional documentation which may be important for proper usage.

Related Documents

Related Information SC5-FESTIVAL	
SC5-FESTIVAL Home	www.ekf.com/s/sc5/sc5.html
SC5-FESTIVAL Product Information	www.ekf.com/s/sc5/sc5_pi.pdf

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

- XEON®, Core™: ® Intel
- CompactPCI, CompactPCI PlusIO, CompactPCI Serial: ® PICMG
- Windows: ® Microsoft
- EKF, ekf system: ® EKF

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

Standards

Reference Documents		
Term	Document	Origin
CompactPCI® Serial	CompactPCI Serial Specification, PICMG® CPCI-S.0	www.picmg.org
DisplayPort	VESA DisplayPort Standard Version, DisplayPort Alt Mode on USB Type-C	www.vesa.org
Ethernet	IEEE Std 802.3 IEEE Std 1588-2008 Precision Time Protocol	standards.ieee.org
HD Audio	High Definition Audio Specification	www.intel.com
LPC	Low Pin Count Interface Specification	www.intel.com
M.2	PCI Express M.2 Specification	www.pcisig.com
NVMe	NVM Express Specification	www.nvmexpress.org
PCI Express®	PCI Express® Base Specification	www.pcisig.com
SATA	Serial ATA Specification	www.sata-io.org
TPM	Trusted Platform Module	www.trustedcomputinggroup.org
UEFI	Unified Extensible Firmware Interface UEFI Specification ACPI Specification	www.uefi.org
USB	Universal Serial Bus Specification, Type-C Cable and Connector Specification Type-C Locking Connector Specification, Universal Serial Bus Power Delivery Specification	www.usb.org

Overview

The SC5-FESTIVAL is a rich featured high performance 4HP/3U CompactPCI® Serial CPU board, equipped with an Intel® Xeon® E3 familiy mobile workstation processor (Kaby Lake Halo platform) for demanding applications. For scalability, the SC5-FESTIVAL is also available with a 7th Generation Intel® Core™ Kaby Lake processor.

The SC5-FESTIVAL front panel is provided with two Gigabit Ethernet jacks, two USB 3.0 receptacles, and two DisplayPort connectors. In addition, up to two USB Type-C front panel receptacles are available as an option, one of them usable alternatively as (third) DisplayPort.

On-board mass-storage solutions are based on low profile mezzanine expansion cards, which accommodate up to two M.2 style SSD modules. One of the M.2 sockets is suitable for a fast NVMe (PCIe Gen3 x 4) module, and the other for a low cost SATA type M.2.

The SC5-FESTIVAL is equipped with up to 32GB DDR4 RAM with ECC support. Up to 16GB memory-down are provided for rugged applications, and another 16GB are available via the DDR4 ECC SO-DIMM socket.

The powerful Xeon® E3-1500 v6 series processor is accompanied by the CM238 mobile PCH, for a maximum of high speed I/O resources (e.g. PCI Express®, SATA, USB). Thus, 22 PCIe lanes are available for backplane use, and up to 8 lanes for local mezzanine expansion.

The SC5-FESTIVAL is provided with an on-board SATA hardware RAID controller, enabling high-capacity mass storage solutions across the CompactPCI® Serial backplane.

As an option, up to eight Gigabit Ethernet Ports are available via the backplane connector P6 (S80-P6 low profile mezzanine expansion card).

Technical Features

Feature Summary

Feature Summary

General

- PICMG® CompactPCI® Serial (CPCI-S.0) CPU card
- Form factor single size Eurocard (board dimensions 100x160mm²)
- Mounting height 3U
- Front panel width 4HP (8HP/12HP assembly with optional mezzanine side card)
- Front panel I/O connectors for typical system configuration (2 x USB3, 2 x DisplayPort, 2 x GbE)
- Backplane communication via PCI Express® Gen3, SATA 6G, USB 3.0, Gigabit Ethernet
- Local mezzanine expansion option, COTS and custom specific boards

Processor

- Intel® Kaby Lake-H mobile platform with ECC (CM238 mobile workstation PCH)

- Intel® Xeon® processor E3 v6 family (mobile workstation)
- Xeon E3 1505M v6 ▪ 3/4GHz ▪ 8M ▪ 4C/8T ▪ DDR4 2400 ECC ▪ 45/35W ▪ GT2 - P630 ▪ vPRO™/AMT
- Xeon E3 1505L v6 ▪ 2.2/3GHz ▪ 8M ▪ 4C/8T ▪ DDR4 2400 ECC ▪ 25W ▪ GT2 - P630 ▪ vPRO™/AMT
- Xeon E3 1501M v6 ▪ 2.9/3.6GHz ▪ 6M ▪ 4C/4T ▪ DDR4 2400 ECC ▪ 45/35W ▪ GT2 - P630 ▪ vPRO™/AMT
- Xeon E3 1501L v6 ▪ 2.1/2.9GHz ▪ 6M ▪ 4C/4T ▪ DDR4 2400 ECC ▪ 25W ▪ GT2 - P630 ▪ vPRO™/AMT

- 7th Generation Intel® Core™ mobile processor
- i3 7100E ▪ 2.9GHz ▪ 3M ▪ 2C/4T ▪ DDR4 2400 ECC ▪ 35W ▪ GT2 - 630
- i3 7102E ▪ 2.1GHz ▪ 3M ▪ 2C/4T ▪ DDR4 2400 ECC ▪ 25W ▪ GT2 -630

Firmware

- Phoenix® UEFI (Unified Extensible Firmware Interface) V2.5 with CSM*
- Phoenix® Release V4.0.1 SCT (SecureCore Technology)
- ACPI 5.0
- Fully customizable by EKF
- Secure Boot and Measured Boot supported - meeting all demands as specified by Microsoft®
- Windows®, Linux and other (RT)OS' supported
- Intel® AMT supported for Intel® Xeon® E3 v6 (disabled by default, must be enabled via BIOS setup)

* CSM (Compatibility Support Module) emulates a legacy BIOS environment, which allows to boot a legacy operating system such as DOS, 32-bit Windows and some RTOS'

Feature Summary

Main Memory

- Integrated memory controller up to 32GB DDR4 2400 +ECC
- DDR4 +ECC soldered memory up to 16GB
- DDR4 +ECC SO-DIMM memory module socket up to 16GB

Graphics

- Integrated graphics engine, 3 symmetric independent displays
- 3D HW acceleration DirectX12, OpenCL 2.x, OpenGL 4.4, ES 2.0
- HW video decode/encode HEVC10b 10-bit, VP9 10-bit, JPEG
- HDR (High Dynamic Range) Rec. 2020 Wide Color Gamut
- High-bandwidth Digital Content Protection (HDCP)
- UHD premium content playback
- Front panel options: Dual DisplayPort (DP) connectors
- 3rd DisplayPort optional via Type-C connector on low profile mezzanine card
- Max resolution 4096 x 2304 @60Hz (any DisplayPort, concurrent operation)
- DisplayPort™ 1.2 Multi-Stream Transport (MST) - display daisy chaining
- MST max resolution via single DP connector 2880x1800@60Hz (2 displays), 2304x1440@60Hz (3 displays)
- Integrated audio (3 independent audio streams)

Networking

- Up to 10 networking interfaces in total - 2 x front RJ45 GbE, mezzanine option 8 x backplane GbE, or 4 x RJ45 or M12-X front panel Ethernet connectors
- 1000BASE-T, 100BASE-TX, 10BASE-T connections (2.5GBASE-T mezzanine option)
- Front port 1 - I219LM with Intel® AMT support
- Front port 2 - Intel® I210-IT -40°C to +85°C GbE NIC w. integrated PHY
- IPv4/IPv6 checksum offload, 9.5KB Jumbo Frame support, EEE Energy Efficient Ethernet
- IEEE 802.1Qav Audio-Video-Bridging (AVB) enhancements for time-sensitive streams
- IEEE 1588 and 802.1AS packets hardware-based time stamping for high-precision time synchronization
- Backplane Gigabit Ethernet option w. S80-P6 mezzanine module - Marvell Peridot switch
- Backplane Gigabit Ethernet option w. S82-P6 mezzanine module - 4 x Intel® I210-IT NIC
- Backplane 2.5GbE option w. S83-P6 mezzanine module - 4 x Intel® I226-IT NIC
- Option front panel 4 x RJ45 2.5GbE ports with SCJ-VEENA side card (8HP F/P width)
- Option front panel 4 x M12-X GbE ports with SCL-RHYTHM side card (8HP F/P width)

Feature Summary

Chipset

- Intel® CM238 Mobile Workstation Platform Controller Hub (PCH)
- PCIe Gen3 8GT/s
- SATA 6G
- USB3
- GbE
- LPC, Audio, Legacy

On-Board Building Blocks

- Additional on-board devices, PCIe® based
- 1 x Gigabit Ethernet controller Intel® I210IT
- 1 x Gigabit Ethernet PHY Intel® I219LM
- IEEE 1588-2008 Precision Time Protocol including PPS and PPM signals supported
- SATA 6G RAID controller Marvell® 88SE9230, ARM powered subsystem for host CPU offload

Security

- Trusted Platform Module
- TPM 2.0 for highest level of certified platform protection
- Infineon Optiga™ SLB 9665 cryptographic processor
- Conforming to TCG 2.0 specification
- AES hardware acceleration support (Intel® AES-NI)

Front Panel I/O (4HP)

- 2 x Gigabit Ethernet RJ45 (1 = PCH & I219LM - iAMT, 2 = I210IT)
- 2 x DisplayPort (from processor integrated HD graphics engine, standard DP latching receptacles)
- 2 x USB 3.0
- Option 2 x Type-C USB 3.1 Gen1 (requires low profile mezzanine expansion card w. front panel I/O)
- Support for Type-C locking plugs (dual screw) according to the 'Locking Connector Spec. Rev. 1.0'
- Option DisplayPort Alt Mode on lower Type-C connector (3rd video monitor output)

Feature Summary

CompactPCI® Serial Backplane Resources

- PICMG® CPCI-S.0 CPU card & system slot controller
- 16 x PCIe Gen3 8GT/s (2 links x 8 for two fat pipe slots, derived directly from the Xeon® or Core™ CPU)
- 6 x PCIe Gen3 8GT/s (6 links x 1 for peripheral slots, derived from CM238 PCH)
- 2 x SATA 6G (from CM238 PCH)
- 4 x SATA 6G (Marvell hardware RAID controller)
- 5 x USB2, 3 x USB3 (from CM238 PCH)
- Backplane Gigabit Ethernet option w. S80-P6 mezzanine module - Marvell Peridot switch
- Backplane Gigabit Ethernet option w. S82-P6 mezzanine module - 4 x Intel® I210-IT NIC
- Backplane 2.5GbE option w. S83-P6 mezzanine module - 4 x Intel® I226-IT NIC

Local Expansion & Mezzanine Mass Storage Options

- Mezzanine side card connectors for optional local expansion
- Low profile mezzanine modules available (4HP front panel) and also side cards (8HP F/P assembly)
- P-EXP - Legacy interface (from PCH)
- P-HSE1 - configurable as 4 x SATA 6G or 4 x PCIe (from CM238 PCH), 1 x USB3
- P-HSE2 - 4 x PCIe (from CM238 PCH) & 3rd DisplayPort (from CPU)

- 4HP Low profile mezzanine module preferred options:
- S20-NVME Mezzanine module - 1 x M.2 2280 NVME SSD socket, 1 x Type-C USB F/P connector
- S40-NVME Mezzanine module - 1 x M.2 2280 NVME SSD socket, 1 x M.2 2280 SATA SSD socket, 2 x Type-C USB F/P Connector (1 connector enabled for DisplayPort alternate mode)
- S48-SSD Mezzanine Module - 2 x M.2 2280 NVME SSD sockets, 1 x USB Type-C
- S80-P6 Mezzanine module - 1 x M.2 2280 NVMe SSD socket, 8 x Gigabit Ethernet via P6 backplane connector (switch based solution)
- S82-P6 Mezzanine module - M.2 NVMe SSD & 4 x GbE NIC via P6 backplane connector
- S83-P6 Mezzanine module - M.2 NVMe SSD & 4 x 2.5GbE NIC via P6 backplane connector
- Custom specific storage & I/O module design

- 8HP/12HP Mezzanine side card options:
- SCJ-VEENA Quad port 2.5GbE NIC, front panel RJ45 jacks, M.2 (NVMe/SATA) SSD
- SCL-RHYTHM Quad port GbE NIC, front panel M12-X receptacles, M.2 (NVMe/SATA) SSD
- SCZ-NVM Dual M.2 NVMe SSD, quad UART
- P01-M12 Replacement for RJ45 GbE jacks by M12-X receptacles
- PCU-P400-UPTEMPO Dual M.2 SATA SSD, HD-Audio, 2 x RS-232, USB2
- Custom specific side card design - I/O and storage

- Special purpose mezzanine side card option:
- SCX-PCIE CompactPCI® Serial backplane doubling
- ECX-PCIE Backplane coupler CompactPCI® Serial to CompactPCI® Express

Feature Summary

Environmental & Regulatory

- Suitable e.g. for industrial, transportation & instrumentation applications
- Designed & manufactured in Germany
- ISO 9001 certified quality management
- Long term availability
- Rugged solution
- Coating, sealing, underfilling on request
- Lifetime application support
- RoHS compliant
- Operating temperature 0°C to +70°C
- Operating temperature -40°C to +85°C (industrial temperature range) on request
- Storage temperature -40°C to +85°C, max. gradient 5°C/min
- Humidity 5% ... 95% RH non condensing
- Altitude -300m ... +3000m
- Shock 15g 0.33ms, 6g 6ms
- Vibration 1g 5-2000Hz
- MTBF 21.2 years
- EC Regulatory EN55035, EN55032, EN62368-1 (CE)

RT OS Board Support Packages & Driver

- LynxOS - on request
- On Time RTOS-32 - on request
- OS-9 - on request
- QNX 4.x, 6.x - on request
- Real-Time Linux (RT Patch) - on request
- RTX - on request
- VxWorks 5.5 & 6.9 - on request
- VxWorks 7.0 - on request
- Others - on request

items are subject to changes w/o further notice


SC5
FESTIVAL

Power Requirements

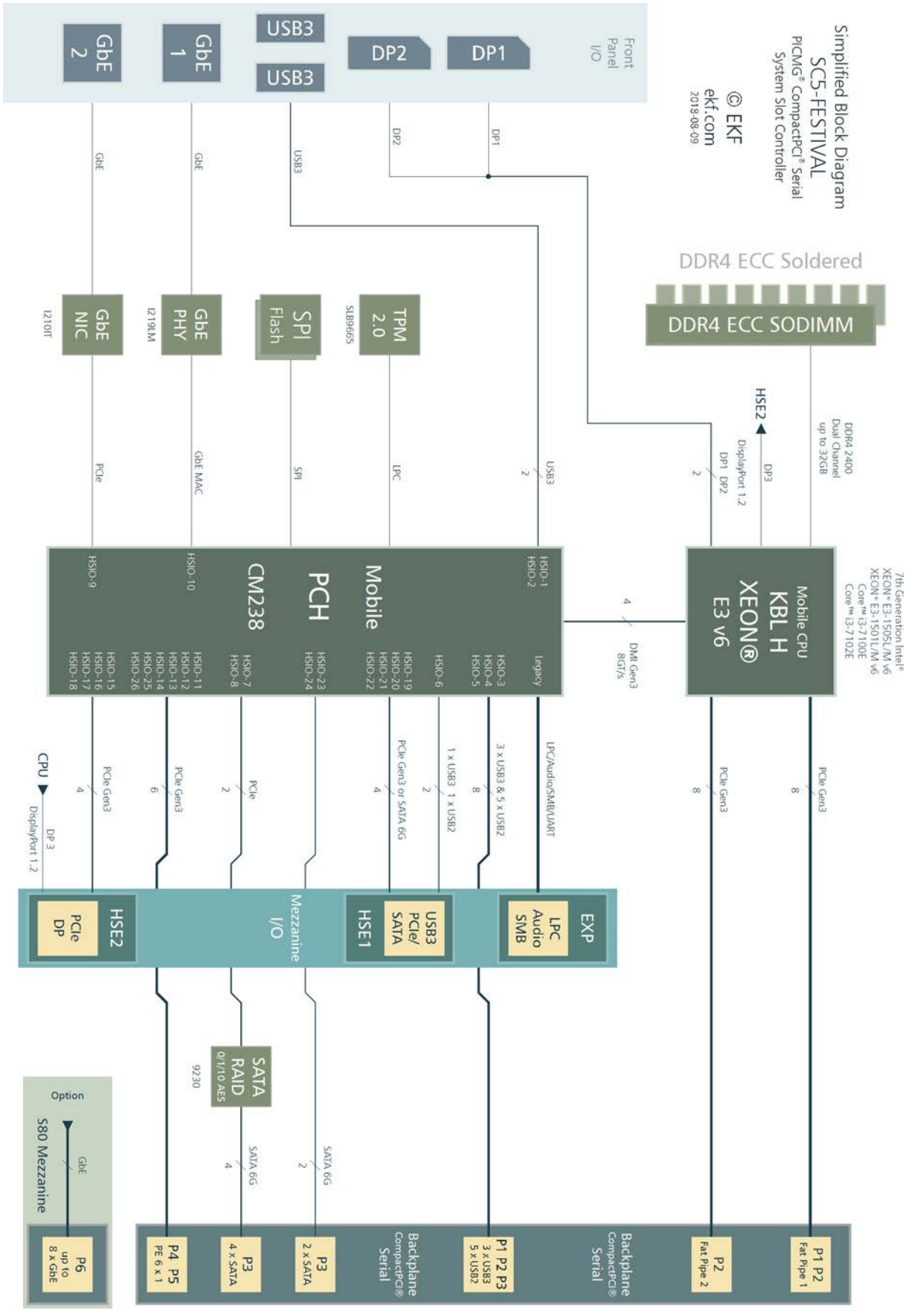
Power Requirements		
Board	Load Current [A] at +12V (±10%)	
	Maximum Performance LFM / HFM / Turbo [1]	Windows 10 Idle LFM / HFM / Turbo [1]
SC5-44XX	1.9 / 2.4 / 2.8 [2]	0.7 / 0.7 / 0.7 [2]
SC5-64XX	2.7 / 4.4 / 5.0 [2]	0.7 / 0.7 / 0.7 [2]
	Load Current [A] at +5V[STDBY] (±10%) [3]	
	Full On / Sleep / Hibernate / Soft Off (S0 / S3 / S4 / S5)	0 / 0 / 0 / 0.1

[1] Intel SpeedStep Frequence Modes LFM: Low Frequency Mode, HFM: High Frequency Mode.

[2] Add 50/140mA (link only/active) @1Gbps per Ethernet Port.

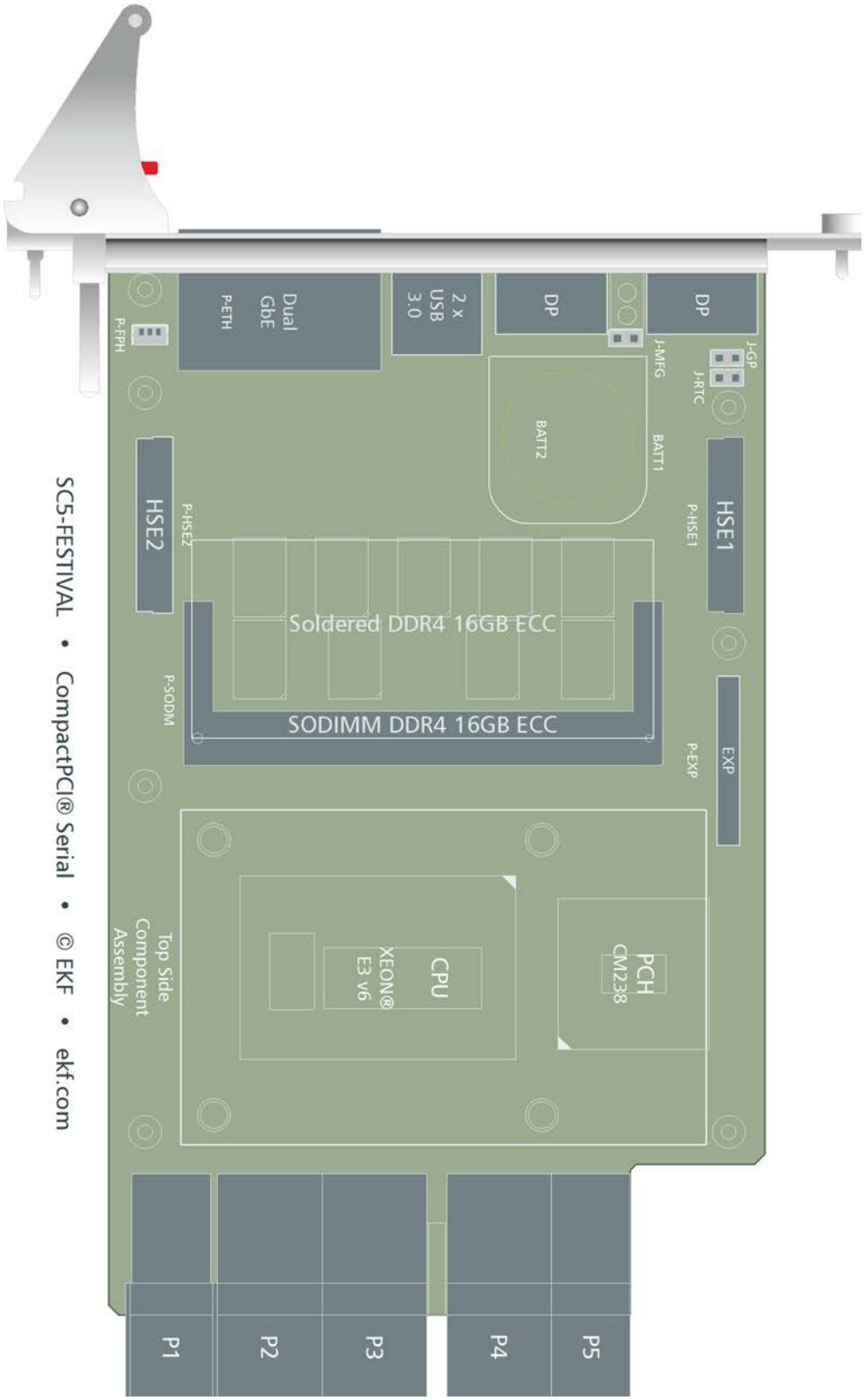
[3] This power supply is optional. It can be left open if not available.

Block Diagram

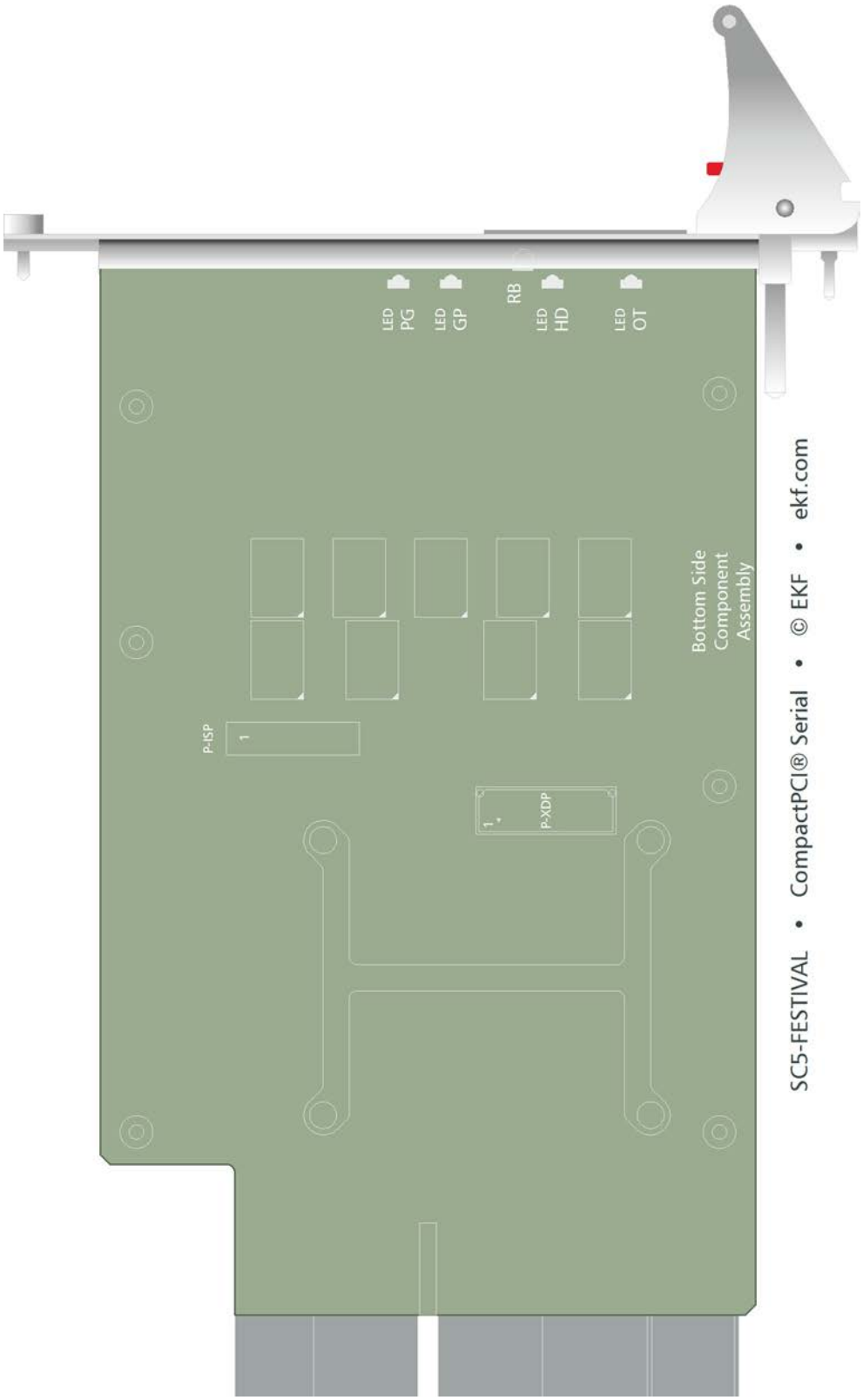


www.ekf.com/s/sc5/img/sc5_blk.pdf

Top View Component Assembly



Bottom View Component Assembly



Front Panel Connectors

ETH 1/2	Dual Gigabit Ethernet RJ-45 receptacles with integrated indicator LEDs
DP 1/2 DP 3	DisplayPort digital video output receptacles Optional with S40-NVME, Type-C receptacle (DP Alt Mode enabled)
USB 1/2 USB 3/4	Universal Serial Bus 3.0 type A receptacles (USB 3.1 Gen1 SuperSpeed 5Gbps) Optional with S40-NVME, two Type-C receptacles (USB 3.1 Gen1 SuperSpeed 5Gbps)

Front Panel Switches & Indicators

FPH	Front Panel Handle with integrated switch (programmable function, power event button by default)
GP	General Purpose bicolour LED
HD	Bicoloured LED indicating any activity on SATA ports
OT	LED indicating CPU over-temperature
PG	Power Good/Board Healthy bicolour LED
RB	System Reset Button (Option)

On-Board Connectors & Sockets

P-EXP	Utility EXPansion Interface Connector (LPC, USB, HD Audio, SMBus), interface to optional side board
P-HSE1	High Speed Expansion Connector 1 (4 x PCIe/SATA, 2 x USB), interface to optional low profile mezzanine module or side board
P-HSE2	High Speed Expansion Connector 2 (4 x PCIe, DisplayPort), interface to optional low profile mezzanine module or side board
P1	CompactPCI® Serial Type A Connector
P2-P4	CompactPCI® Serial Type B Connectors
P5	CompactPCI® Serial Type C Connector
P6	Option only with S80-P6 low profile mezzanine module, CompactPCI® Serial Type D Connector
P-SODM	260-pin DDR4 ECC Memory Module (ECC SODIMM)
P-XDP	CPU Debug Port [1)]

[1)] Connector populated on customers request only

Pin Headers

P-FPH	Pin header suitable for Front Panel Handle switch cable harness
P-ISP	PLD glue logic device programming connector, not populated

Jumpers

J-GP	Jumper to reset UEFI/BIOS Setup to EKF Factory Defaults, IEEE 1588 Pulse per Second Output
J-MFG	Jumper to enter Manufacturing Mode, not populated
J-RTC	Jumper to reset RTC circuitry (part of PCH), not populated

Microprocessor

The SC5-FESTIVAL is equipped with a member of the 7th generation Intel® processor family: XEON® processor E3 v6 or Core™ processor (code name Kaby Lake H). These dual/quad core low power processors provide integrated graphics and memory controller, which results in a very efficient platform design.

The processors supported by the SC5-FESTIVAL are SKUs with a thermal design power (TDP) of 25-45W. Due to the cTDP feature (configurable TDP) the power consumption of the 45W parts may be lowered by UEFI setup to fit the customers requirements (see table below). The processors are housed in a Micro FC-BGA package for direct soldering to the PCB, i.e. the chip cannot be removed or changed by the user.

The processors are running at core clock base speeds up to 3GHz. Due to Enhanced Intel® SpeedStep® and Intel® Turbo Boost Technology each core can decrease or increase its nominal operating frequency in a range from 800MHz up to 4GHz. The clock speed is chosen depending on several parameters like the power states of the processor cores/graphics engine, the currently required performance, the actual core temperature etc.

Power is applied across the CompactPCI® connector P1 (12V). The processors core voltage are generated by a switched voltage regulator according to Intels IMVP-8 voltage regulator specification.

Intel® XEON®/Core™ Processors Supported [1]									
Processor Number	Physical/ Logical Cores	Core Clock nom/max [GHz]	Cache [MB]	Gfx Clock [MHz]	Junction Temp. [°C]	TDP [W]	CPU ID	Stepping	SPEC Code
E3-1505L v6	4/8	2.2/3	8	1000	100	25	0x906E9	B-0	SR34X
E3-1505M v6 [2]	4/8	3/4	8	1100	100	45/35	0x906E9	B-0	SR32K
E3-1501L v6	4/4	2.1/2.9	6	1000	100	25	0x906E9	B-0	
E3-1501M v6 [2]	4/4	2.9/3.6	6	1000	100	45/35	0x906E9	B-0	
i3-7100E	2/4	2.9/-	3	950	100	35	0x906E9	B-0	SR34V
i3-7102E	2/4	2.1/-	3	950	100	25	0x906E9	B-0	SR34W

[1] The processors listed are units with long life support.
[2] This processor may run with different TDPs configurable by UEFI settings.

Thermal Considerations

In order to avoid malfunctioning of the SC5-FESTIVAL, take care of appropriate cooling of the processor and system, e.g. by a cooling fan suitable to the maximum power consumption of the CPU chip actually in use. The processor contains digital thermal sensors (DTS) that are readable via special CPU registers or via PECI bus. DTS allows to get the temperatures of each CPU core separately.

Two further temperature sensors, one of it located in the system hardware monitor NCT7491, allows for acquisition of the boards surface temperature and the thermal state of the onboard system memory channel. Beside this the NCT7491 also keeps a PECI 3.0 master for CPU DTS monitoring and supervises most of the supply voltages. A suitable software on Microsoft Windows® systems to display both, the temperatures as well as the supply voltages, is Speedfan, which can be downloaded from the web. After installation, both temperatures and voltages can be observed permanently from the Windows® taskbar.

The SC5-FESTIVAL is equipped with a passive heatsink. Its height takes into account the 4HP limitation in mounting space of a CompactPCI® board. In addition, a forced vertical airflow through the system enclosure (e.g. bottom mount fan unit) is strongly recommended ($>20m^3/h$ or 2m/s (400LFM) around the CPU slot). Be sure to thoroughly discuss your actual cooling needs with EKF. Generally, the faster the CPU speed the higher its power consumption. For higher ambient temperatures, consider increasing the forced airflow to 3m/s (600LFM) or more.

The table showing the supported processors above give also the maximum power consumption (TDP) of a particular processor. Fortunately, the power consumption is by far lower when executing typical Windows® or Linux tasks. The heat dissipation increases when e.g. rendering software like the Acrobat Distiller is executed.

The processors support Intel's Enhanced SpeedStep® technology. This enables dynamic switching between multiple core voltages and frequencies depending on core temperature and currently required performance. The processors are able to reduce their core speed and core voltage in multiple steps down to 800MHz. Additional a reduction of the graphics core clock (down to 350MHz) and voltage is possible. This leads to an obvious reduction of power consumption resulting in less heating.

A further way to reduce power consumption is achieved by Intels voltage regulators belonging to the IMVP8 standard. These regulators allows the processor to regulate the voltages to the cores, graphics, system agent and other units separately depending on their performance needs. Parts that are currently idle may switched off to save power.

Main Memory

The SC5-FESTIVAL features two channels of DDR4 SDRAMs with support of ECC (Error Correction Code). One channel is realized with 18 memory devices soldered to the board (Memory Down) and delivers a capacity of up to 16GB with a clock frequency of 2400MHz (PC4-2400).

The 2nd channel provides a socket for installing a 260-pin ECC SODIMM module thus allowing a simple expansion of system memory (max. module height = 1.25 inch). Supported are unbuffered DDR4 ECC SODIMMs (72-bit) with V_{DD}=1.2V featuring on-die termination (ODT), according the PC4-2400 specification. Minimum module size is 4GB; maximum module size is 16GB. Please note that DDR4 without the ECC feature will not work on SC5-FESTIVAL.

It is recommended to add a SODIMM module with same size as the Memory Down to get best performance. Since some of the system memory is dedicated to the graphics controller a typically development of 2x8GB of memory is recommended to run operating systems like Windows® 10 or Linux.

The memory controller supports symmetric and asymmetric memory organization. The maximum memory performance can be obtained by using the symmetric mode. When in this mode, the memory controller accesses the memory channels in an interleaved way. Since the processors support Intels Flex Memory Technology, interleaved operation isn't limited to systems using memory channels of equal capacity. In the case of unequal memory population the smaller memory channel dictates the address space of the interleaved accessible memory region. The remainder of the memory is then accessed in non-interleaved mode.

In asymmetric mode the memory always will be accessed in a non-interleaved manner with the drawback of less bandwidth. The only meaningful application of asymmetric mode is the special case when only one memory channel is populated (i.e. the SODIMM socket may be left empty).

The contents of the SPD EEPROM on the SODIMM is used by the UEFI/BIOS at POST (Power-on Self Test) to get any necessary timing parameters to program the memory controller within the chipset.

Graphics Subsystem

The graphics subsystems main interfaces like DisplayPort and DVI are part of the processor. Only a few sideband signals (DDC channel, hot plug detection) are located within the PCH CM238.

The SC5-FESTIVAL offers two DisplayPort interfaces with latching receptacle in the front panel. The latching feature prevents DisplayPort cables from detaching in vibrating or harsh environments.

A 3rd DisplayPort is fed to the on-board connector P-HSE2. EKF expansion boards like S40-NVME feature the possibility to gain access to the 3rd DisplayPort interface via Type-C receptacle.

When alternate display interfaces like DVI-I or VGA are required, a variety of converters are available in active or passive form, as adapters or cables.

Independent from the video standard actually in use, DisplayPort, DVI-I or VGA, the VESA DDC standard is supported. This allows to read out important parameters, e.g. the maximum allowable resolution, from the attached monitor. DDC power, +3.3V on DisplayPort connectors, is delivered via electronic switches to protect the board from an external short-circuit condition (1.5A) and to prevent back current flows.

Graphics drivers can be downloaded from the Intel web site.

LAN Subsystem

The Ethernet LAN subsystem is composed of two Gigabit Ethernet ports: One Intel i219LM Physical Layer Transceiver (PHY) using the PCH CM238 internal MAC and one Intel i210IT Gigabit Ethernet Controller. These devices provide also legacy 10Base-T and 100Base-TX connectivity. These Ethernet ports are fed to two RJ45 jacks located in the front panel. Each port includes the following features:

- One PCI Express lane per Ethernet port (250MB/s)
- 1000Base-Tx (Gigabit Ethernet), 100Base-TX (Fast Ethernet) and 10Base-T (Classic Ethernet) capability.
- Half- or full-duplex operation.
- IEEE 802.3u, 802.3ab Auto-Negotiation for the fastest available connection.
- Jumperless configuration (complete software-configurable).

Two bicoloured LEDs integrated into the dedicated RJ-45 connector in the front panel are used to signal the LAN link, the LAN connection speed and activity status.

Each device is connected by a single PCI Express lane to the PCH. Their MAC addresses (unique hardware number) are stored in dedicated FLASH/EEPROM components. The Intel Ethernet software and drivers for the i219LM and i210IT are available from Intel's World Wide Web site for download.

When managing the board by Intel Active Management Technology (iAMT), the dedicated network port to do so is accessible by the RJ45 connector GbE1 (the upper port within the front panel).

The i210 controller supports the IEEE 1588 Precision Time Protocol (the one connected to the lower port within the front panel (GbE2)) and is capable to generate Pulse per Second (PPS) and Pulse per Minute (PPM) signals that may be routed to the jumper J-GP and the CompactPCI® Serial connector P1. These signals can be used to trigger events on Mezzanine Side Boards or Peripheral Boards. The following routing is possible by UEFI/BIOS settings:

- Pulse per Second (PPS): J-GP Pin 1 and CompactPCI® Pin J3 (signal SATA-SCL)
- Pulse per Minute (PPM): CompactPCI® Pin H3 (signal SATA-SDO)

Serial ATA Interface (SATA)

The SC5-FESTIVAL provides a total of up to ten serial ATA (SATA) ports, derived from up to three independent SATA controllers. All of these ports support data transfer rates of 6Gbps (600MB/s), 3Gbps (300MB/s) or 1.5Gbps (150MB/s). SATA controllers are located within the CM238 Platform Controller Hub that holds up to 6 SATA interfaces (depends on the configuration on expansion interface P-HSE1) and in a separate SATA host controller Marvell 88SE9230, providing four SATA ports, all 6Gbps capable.

Up to four of the CM238 ports are fed to the high speed expansion connector P-HSE1. This connector allows the installation of low profile expansion boards like C41-CFAST or C42-SATA to attach the popular CFast cards or Micro SATA SSDs (1.8-inch) respectively. Another mezzanines are the C47-MSATA and C48-M2, carriers for two MSATA or M.2 SSD modules, respectively.

The Marvell 88SE9230 is a SATA 6Gbps AHCI/RAID I/O controller connected via two PCI Express lanes (1GB/s) to the CM238. It supports hardware RAID levels 0, 1 and 10. All of its SATA ports as well as further two CM238 ports are used to supply the CompactPCI® Serial SATA interfaces on the backplane.

A LED named HD located in the front panel, signals disk activity status of any CM238 SATA devices (green) or 88SE9230 devices (yellow).

Additionally a variety of side cards is available, suitable for mounting on the SC5-FESTIVAL in a 4HP (20.32mm) distance (resulting in 8HP front panel width for the assembly). Some of these side boards can accommodate a SATA drive, e.g. a 2.5-inch SSD.

Available for download from Intel's web site are drivers for popular operating systems, e.g. Windows® 8, Windows® 10 and Linux.

Drivers and software to manage the RAID configuration of the 88SE9230 (Windows® application) is provided by Marvell and can be downloaded from EKF’s website.

PCI Express® Interface

The SC5-FESTIVAL is provided with several PCI Express (PCIe) lanes for I/O expansion. Sixteen PCI Express lanes, originating from the processor, are building the two fat pipes defined by CompactPCI® Serial. These two links consists of eight lanes with transfer rates of up to 8Gbps (PCI Express Gen 3).

The CM238 offers a total of up to sixteen PCI Express ports supporting PCIe Gen 3 speed (8GT/s). Four of them are used to operate the two Ethernet Controllers (i219LM and i210IT) and to build a double lane link to the Marvell 88SE9230. Six ports are connected to the CompactPCI® Serial connectors P4/P5 (six lanes), four to the high speed expansion connector P-HSE2.

Four combo ports are fed to the local expansion interface connector P-HSE1, that may work as PCIe (1x4 or 2x2) or as SATA ports, strapped dynamically by configuration signals on P-HSE1. Possible settings are

- One PCIe link x 4
- Two PCIe links x 2
- Four SATA links
- One PCIe link x 2, two SATA links

By default the PCIe lanes connected to the 2nd high speed expansion connector P-HSE2 build four PCIe links with one lane. Alternative configurations (1x4 or 2x2) are possible by programming soft-straps within the SC5 firmware image. Ask EKF if changes are required.

See sections “P-HSE1" and “P-HSE2" from “Mezzanine Connectors" for details.

Universal Serial Bus (USB)

The SC5-FESTIVAL is provided with fourteen USB ports. All of them are USB 2.0 capable, but six ports are also supporting the USB 3.0 SuperSpeed standard. Two USB 3.0 interfaces are routed to front panel connectors, three SuperSpeed ports are feed to the CompactPCI® Serial connectors P1 and P3, one is connected to P-HSE1 interface.

The USB 2.0 interfaces are distributed to the front panel (two ports), two to the high speed expansion connector P-HSE1, and six ports are available across the backplane connectors for CompactPCI® Serial.

The front panel USB connectors can source a minimum of 1.5A/5V each, over-current protected by two electronic switches. Protection for the USB ports on the expansion interface P-HSE1 and on the CompactPCI® Serial connectors is located on expansion boards and the boards on the CompactPCI® Serial backplane respective. The USB xHCI controllers handling the USB port operation at SuperSpeed, high-speed, full-speed and low-speed are integrated into the CM238 PCH.

An xHCI driver (USB 3.0) for Windows® is provided by Intel and can be downloaded from EKF's website.

Utility Interfaces

Besides the high speed mezzanine interface connectors P-HSE1 and P-HSE2, the SC5-FESTIVAL is provided with the utility interface expansion connector socket P-EXP. This connector comprises several interfaces, which may be useful for system expansion on mezzanine cards, as an option:

- HD Audio
- LPC (Low Pin Count)
- I^2C
- 2 x UART (TTL)

The I^2C is connected to controller $I^2C[0]$ of the CM238 platform controller hub. The I^2C signal lines on the P-EXP utility expansion connector are also routed to P-HSE2.

The HD Audio port requires an additional audio codec, as provided e.g. on the SCS-TRUMPET side card.

The LPC bus presents an easy way to add legacy interfaces to the system. EKF offers a variety of mezzanine expansion boards (side cards), to be attached on top of the SC5-FESTIVAL, featuring all classic Super-I/O functionality, for example the SCS-TRUMPET or PCS-BALLET. Access to the connectors PS/2 (mouse, keyboard), COM, USB and audio in/out is given directly from the front panel.

Real-Time Clock

The SC5-FESTIVAL has a time-of-day clock and 100-year calendar, integrated into the CM238 PCH. A battery on the board keeps the clock current when the computer is turned off. The SC5-FESTIVAL uses a holder to keep a CR2032 lithium coin cell, giving an autonomy of more than 5 years. Under normal conditions, replacement should be superfluous during lifetime of the board.

Alternately a CR2032 battery can be soldered in the board when board coating or shock/vibration is an interest.

In applications were the use of a battery is not permitted, a SuperCap can be soldered instead of the battery.

It is also possible to use the SC5-FESTIVAL without any battery or SuperCap. In this case the Real-Time Clock can't keep its time and date. Per default an error message is reported by the UEFI/BIOS during boot in all cases, where the Real-Time clock settings are bad:

```
00C08270: Real Time Clock Error - Check Date and Time settings

00C08251: System CMOS Checksum bad
```

To suppress this message a setup node exists within the UEFI/BIOS (Build #132 or later):

- After Power-On press function key <F2> to enter setup menu
- Advanced→Advanced Menu→Miscellaneous Options→Ignore Battery Error→Enabled
- Advanced→Advanced Menu→Management Engine Configuration→ME Unconfig on RTC Clear →Disabled

SPI Flash

The UEFI/BIOS and iAMT firmware is stored in flash devices with Serial Peripheral Interface (SPI). Up to 16MByte of UEFI code, firmware and user data may be stored nonvolatile in these SPI Flashes.

The SPI Flash contents can be updated by an UEFI Shell, DOS or Linux based tool. This program and the latest SC5-FESTIVAL UEFI/BIOS binary are available from the EKF website. Read carefully the enclosed instructions. If the programming procedure fails e.g. caused by a power interruption, the SC5-FESTIVAL may no more be operable. In this case you would possibly have to send in the board, because the Flash device is directly soldered to the PCB and cannot be changed by the user.

Reset

The SC5-FESTIVAL is provided with several supervisor circuits to monitor supply rails like the CPU core voltage, 1.2V, 3.3V or 5V.

To force a manual board reset, the SC5-FESTIVAL offers a small tactile switch within the front panel. This push-button is indent mounted and requires a tool, e.g. a pen to be pressed, preventing from being inadvertently activated.

The handle within the front panel contains a micro switch that is used to generate a power button event. By pressing the handle's red push button a pulse is triggered.
Animated GIF: www.ekf.com/c/ccpu/img/reset_400.gif

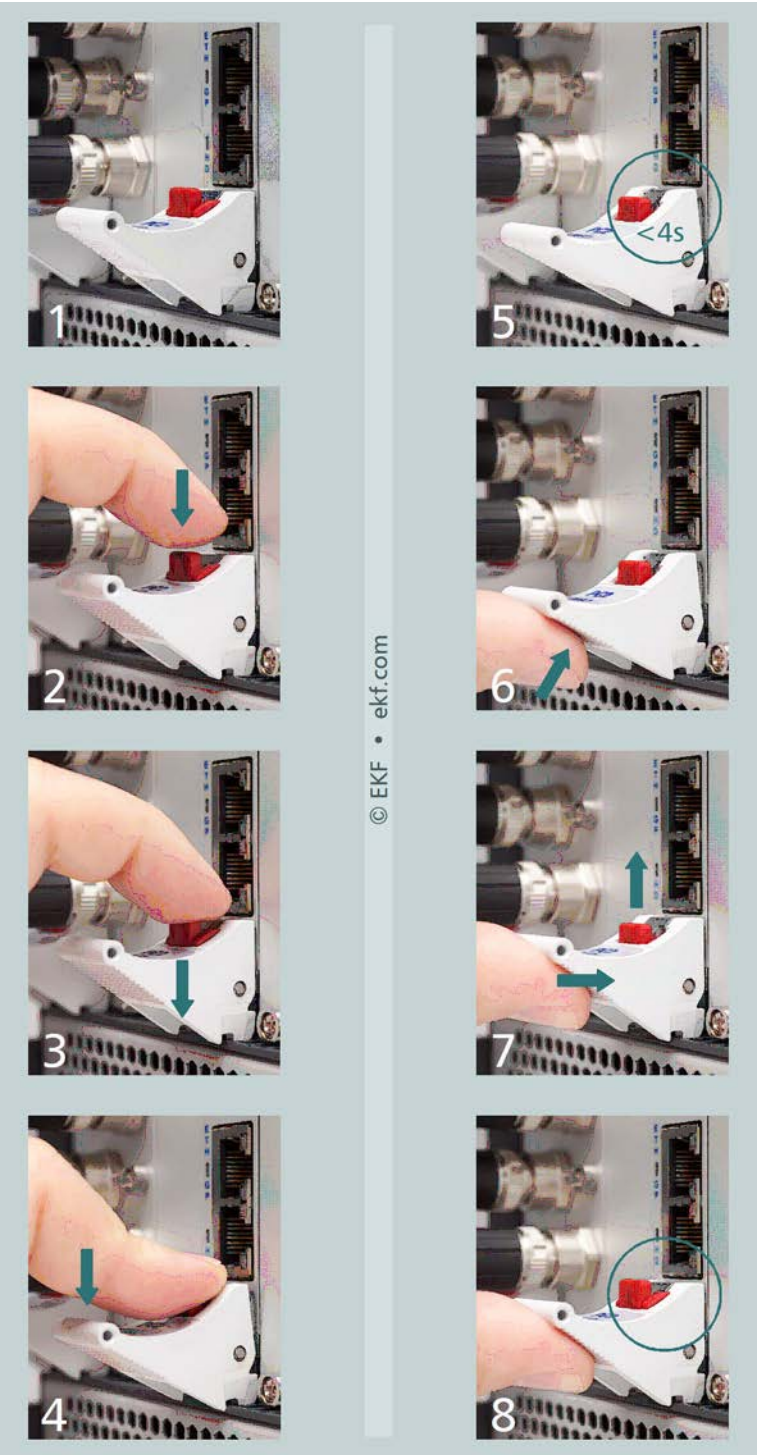
NOTE: To prevent the board to cause a power button override, the handle should be closed immediately after unlocking the front panel handle. A power button override is triggered by opening the front panel handle for at least 4 seconds, which results in bringing the board to power state S5. In case of entering this state, unlock and lock the front panel handle a 2nd time to reenter normal power state S0 again. See also section 'PG (Power Good) LED' to see how the SC5-FESTIVAL indicates the different power states.

WARNING: The SC5-FESTIVAL will enter the power state S5 if the front panel handle is not closed properly when the system powers up. An open handle is signalled by a yellow blinking ‘PG LED’.

The manual reset push-button and the power button functionality of the front panel handle could be passivated by UEFI/BIOS settings.

An alternative (and recommended) way to generate a system reset is to activate the signal PRST# located on CompactPCI® Serial connector P1 pin H2. Pulling this signal to GND will have the same effect as to push the tactile reset switch.

The healthy state of the SC5-FESTIVAL is indicated by the LED PG (Power Good) located in the front panel. This bicoloured LED signals different states of the board (see section below). As soon as this LED begins to lite green, all power voltages are within their specifications and the reset signal has been deasserted.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Watchdog

An important reliability feature is a software programmable watchdog function. The SC5-FESTIVAL contains two of these watchdogs. One is part of the CM238 PCH and also known as TCO Watchdog. A detailed description is given in the CM238 data sheet. Operating systems like Linux offer a driver interface to the TCO watchdog.

The behaviour of the 2nd watchdog is defined within a PLD of the SC5-FESTIVAL, which activates/deactivates the watchdog and controls its time-out period. The time-out delay is adjustable in the steps 2, 10, 50 and 255 seconds. After programming the time-out value and arming the WD, the related software (e.g. application program) must trigger the watchdog periodically. For details on programming the watchdog see section "Board Control and Status Register (BCSR)".

This watchdog is in a passive state after a system reset. There is no need to trigger it at boot time. The watchdog is activated on the first trigger request. If the duration between two trigger requests exceeds the programmed period, the watchdog times out and a full system reset will be generated. The watchdog remains in the active state until the next system reset. There is no way to disable it once it has been put on alert, whereas it is possible to reprogram its time-out value at any time.

Front Panel LEDs

The SC5-FESTIVAL is equipped with four LEDs which can be observed from the front panel. Three of these LEDs are labelled according to their primary meaning, but should be interpreted altogether for system diagnosis:

LED			Status
PG Green/Red	GP Green/Red	HD Green/Yellow	
OFF	GREEN	GREEN	Sleep State S5 (Soft Off)
OFF	GREEN	OFF	Sleep State S4 (Suspend to Disk/Hibernate)
OFF	OFF	GREEN	Sleep State S3 (Suspend to RAM/Standby)
GREEN	RED BLINK	X	After Reset
GREEN	X	X	Board Healthy and in S0 State
YELLOW BLINK	X	X	Front panel handle is unlocked
RED	X	X	Hardware Failure - Power Fault
RED BLINK	X	X	Software Failure

PG (Power Good) LED

The SC5-FESTIVAL offers a bicolour LED labelled PG located within the front panel. After system reset, this LED defaults to signal different power states:

- Off Sleep state S3, S4 or S5
- Green Healthy
- Yellow blink Front panel handle open
- Red steady Hardware failure
- Red blink Software failure

To enter the PG LED state Software Failure, the bit PGLED in the board control register CTRLL_REG must be set. The PG LED remains in this red blinking state until this bit is cleared. After that it falls back to its default function.

GP (General Purpose) LED

This programmable bicolour LED can be observed from the SC5-FESTIVAL front panel. The status of the red part within the LED is controlled by the GPP_D11 of the PCH CM238. Setting GPP_D11 to "1" will switch on the red LED. Turning on or off the green LED is done by setting the bit GPLED in the board control register CTRLH_REG.

The GP LED is not dedicated to any particular hardware or firmware function with exception of special power states of the LED PG as described above. Nevertheless, a red blinking GP LED is an indication that the UEFI/BIOS code couldn't start.

While the CPU card is controlled by the UEFI/BIOS firmware, the GP LED is used to signal board status information during POST (Power On Self Test). After successful operating system boot, the GP LED may be freely used by customer software. For details please refer to www.ekf.com/s/sc5/firmware/fwinfo.txt.

HD (Hard Disk Activity) LED

The SC5-FESTIVAL offers a bicoloured LED marked as HD placed within the front panel. This LED, when blinking green, signals activity on any device attached to the SATA ports of the CM238.

The yellow part of the HD LED shows activity on any of the 88SE9230 SATA ports.

As previously described, the green part of this LED may change its function dependent on the state of the LED PG.

OT (Processor Hot) LED

The thermal status of the processor can be monitored exactly by several utilities that are available in the market (e.g. “Speedfan” for Windows® or “lmsensors” for Linux). The LED “OT” (over-temperature) can be assumed as a summery of that. It shows when the processor impends to get too hot, resulting in reducing its performance by Intel® Speed Step® or similar.

Main Power Supply Control (PS_ON#)

The SC5-FESTIVAL draws its power from the +12V main supply rail defined by the CompactPCI® Serial specification. The board has been designed to control this main power supply by use of the signal PS_ON# (connector P1 pin E2). If the system enters the sleep state S5 (soft off), the signal PS_ON# is pulled high, hence the main power supply is switched-off. The SC5-FESTIVAL is held in soft off state until a power management event (e.g. power button event triggered by the front panel handle) brings back the system to the S0 state.

In order to work as described above and to generate clean signals on PS_ON#, the stand-by voltage +5VSTB is necessary. This optional power rail, tied to connector P1 pin B1, is also part of the CompactPCI® Serial specification. The stand-by power rail must be switched-on "always", independent of the state of PS_ON#.

Nevertheless, +5VSTB is not mandatory to operate the SC5-FESTIVAL. If no stand-by power is available, the board creates this voltage from the main power rail. In this case it is important that the PS_ON# signal is pulled down somewhere in the system.

Power Supply Status (PWR_FAIL#)

Power supply failures may be detected before the system crashes down by monitoring the signal PWR_FAIL#. This active low line (connector P1 pin F3) is an addition to the CompactPCI® Serial specification and may be driven by the power supply. PWR_FAIL# signals the possible failure of the main supply voltage +12V. On the SC5-FESTIVAL the signal PWR_FAIL# is routed to GPP_D0 of the CM238 PCH to analyse the state of the power supply unit.

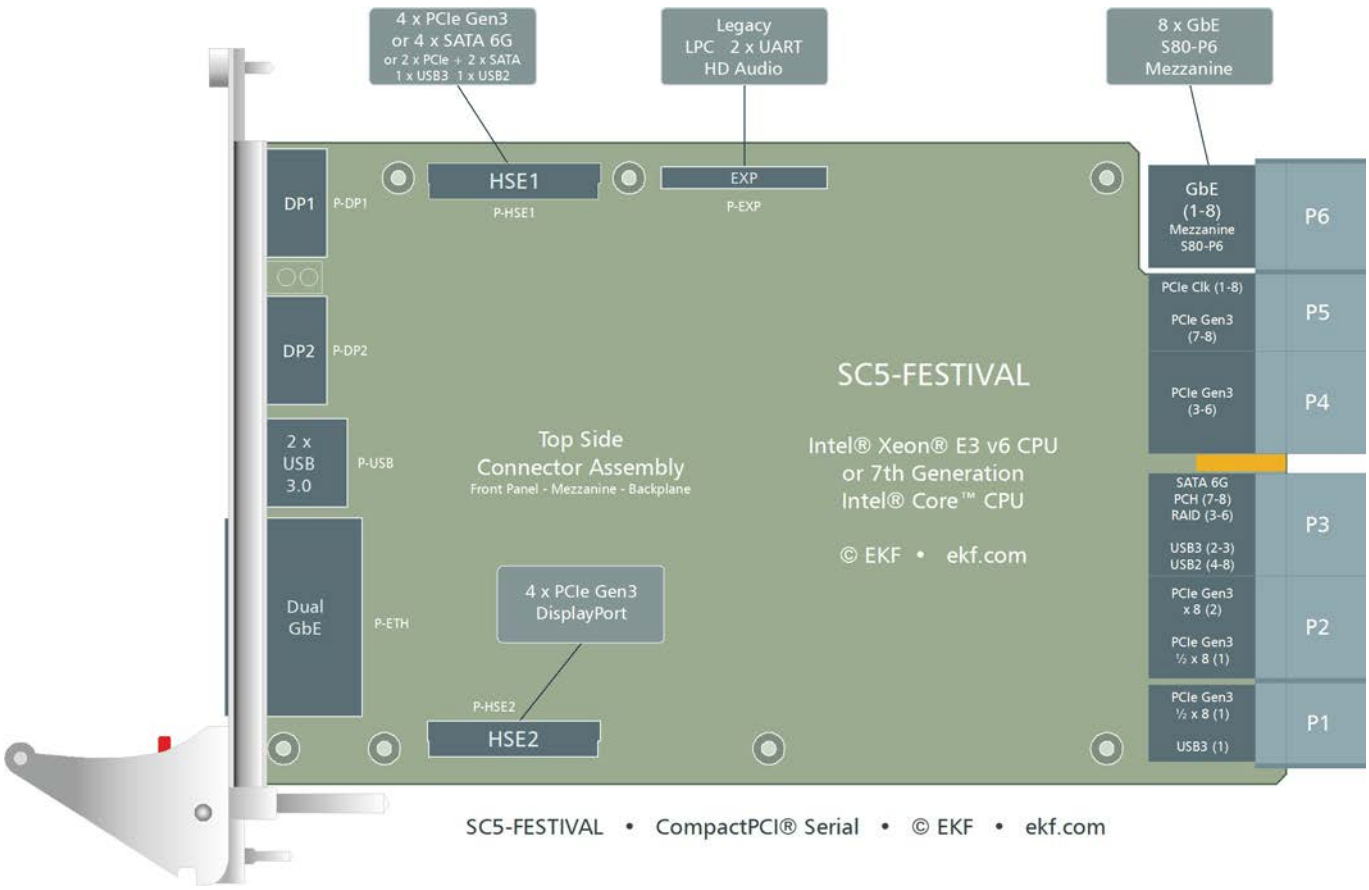
Mezzanine Side Board Options

The SC5-FESTIVAL is equipped with a set of high-speed local expansion interface connectors, which can be optionally used to attach either a low profile mezzanine module (fits into the 4HP front panel envelope) or a side board for an 8HP or even 12HP assembly in total.

The connectors HSE1 and HSE2 are high speed connectors, as required for PCI Express® Gen3 and SATA 6G. The socket EXP is used as a legacy interface (e.g. HD Audio, LPC) and not required for many mezzanine modules. All connectors allow board-to-board heights of 9.5mm (C4* series), 10.0mm (S20, S40), 10.8mm (S60, S80), and 18.7mm (SC* side cards 8HP assembly).

HSE1 can be configured for either 4 x PCIe or 4 x SATA, or 2 x PCIe and 2 x SATA, thanks to the flexible HSIO channels of the CM238 PCH. When HSE1 has been setup for SATA, the SC5-FESTIVAL can be combined e.g. with low cost SSD mass storage mezzanine modules such as the C47-MSATA (dual mSATA carrier) or C48-M2 (dual M.2 SATA sockets). For high performance NVMe based SSD mezzanine modules (S20/40/80), HSE1 must be configured as PCIe x 4.

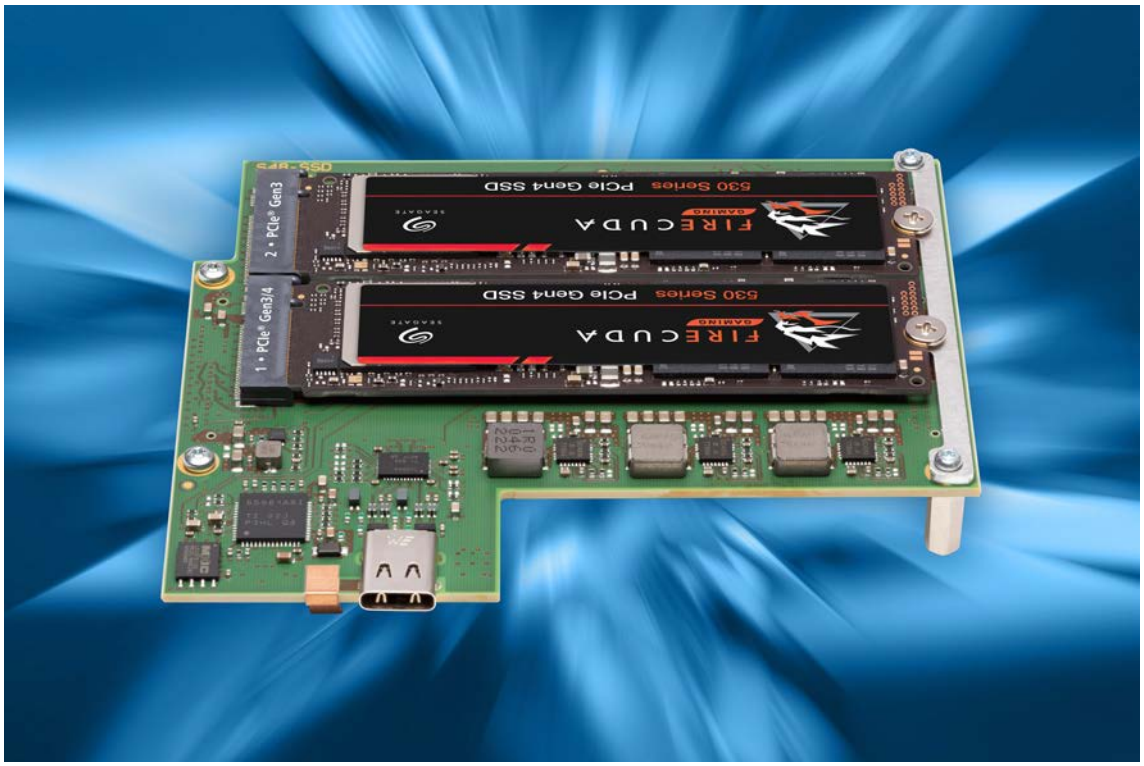
HSE2 is assigned to 4 x PCIe, and in addition the 3rd DisplayPort video output. While S20 and S60 get along with HSE1 only, the S40 and S80 mezzanine modules depend on both HSE1 and HSE2, for additional I/O.



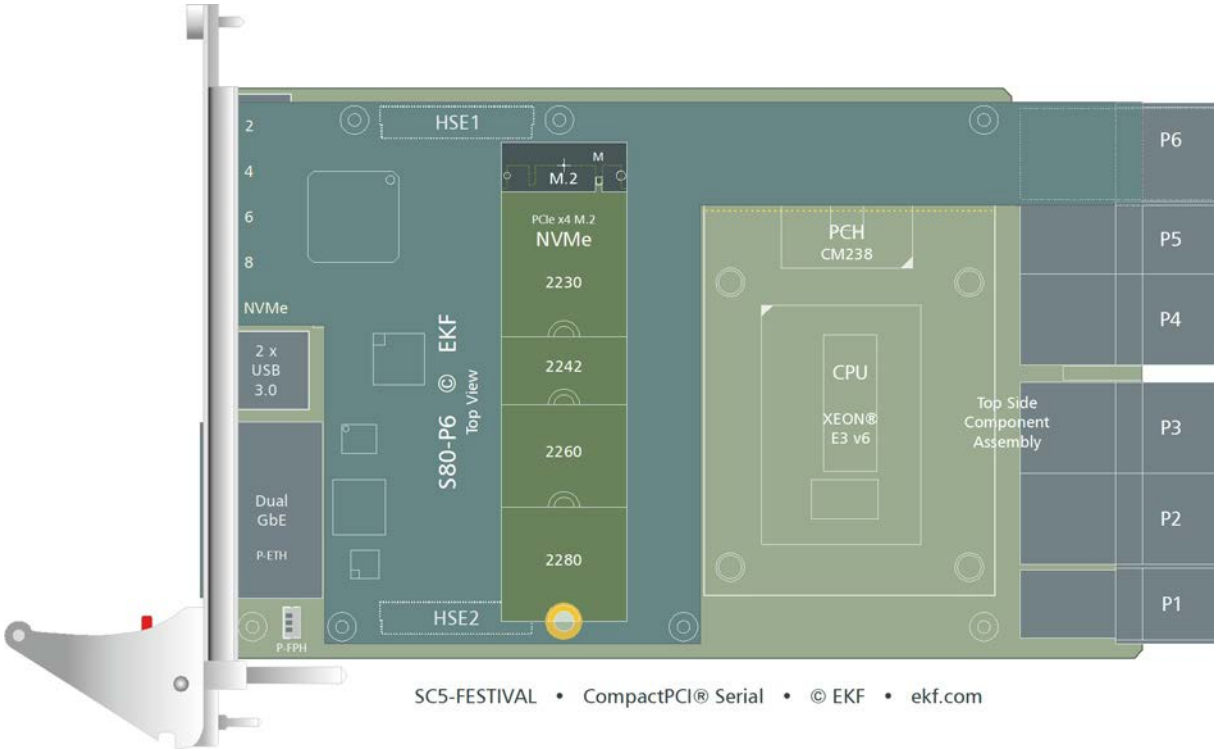
SC5-FESTIVAL • Connector Assembly

SC5-FESTIVAL w. S40-NVME Low Profile Mezzanine

SC5-FESTIVAL 8HP Assy w. S40-NVME & P01-M12

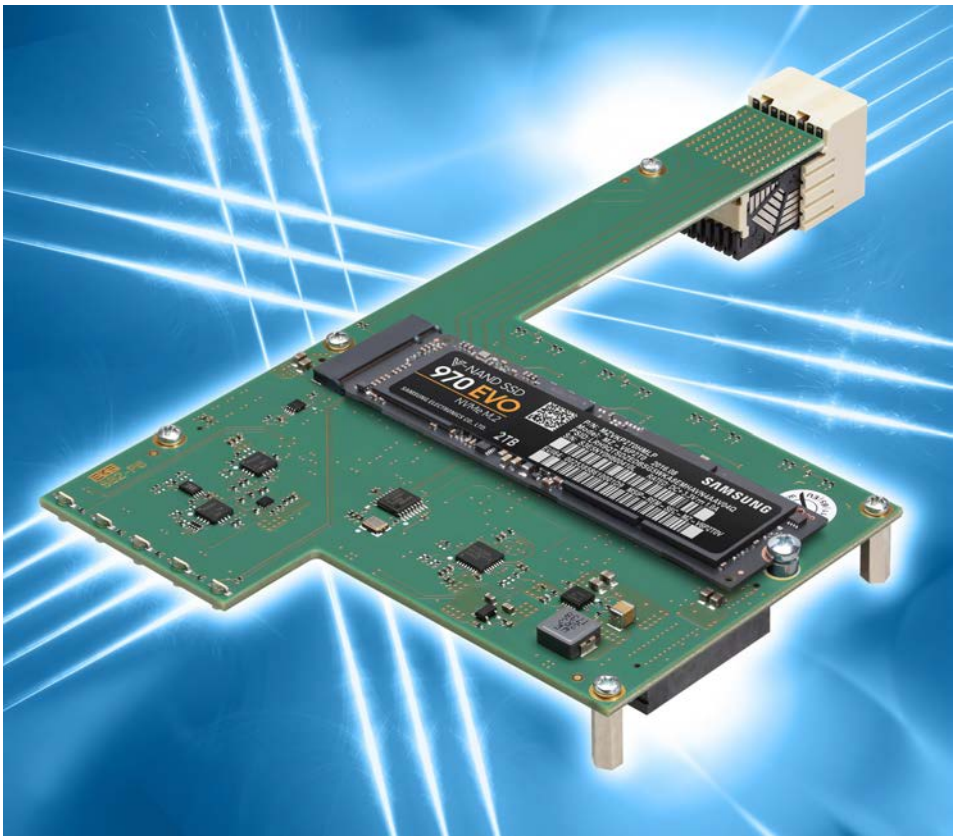


S48-SSD • Dual M.2 NVMe Mass Storage

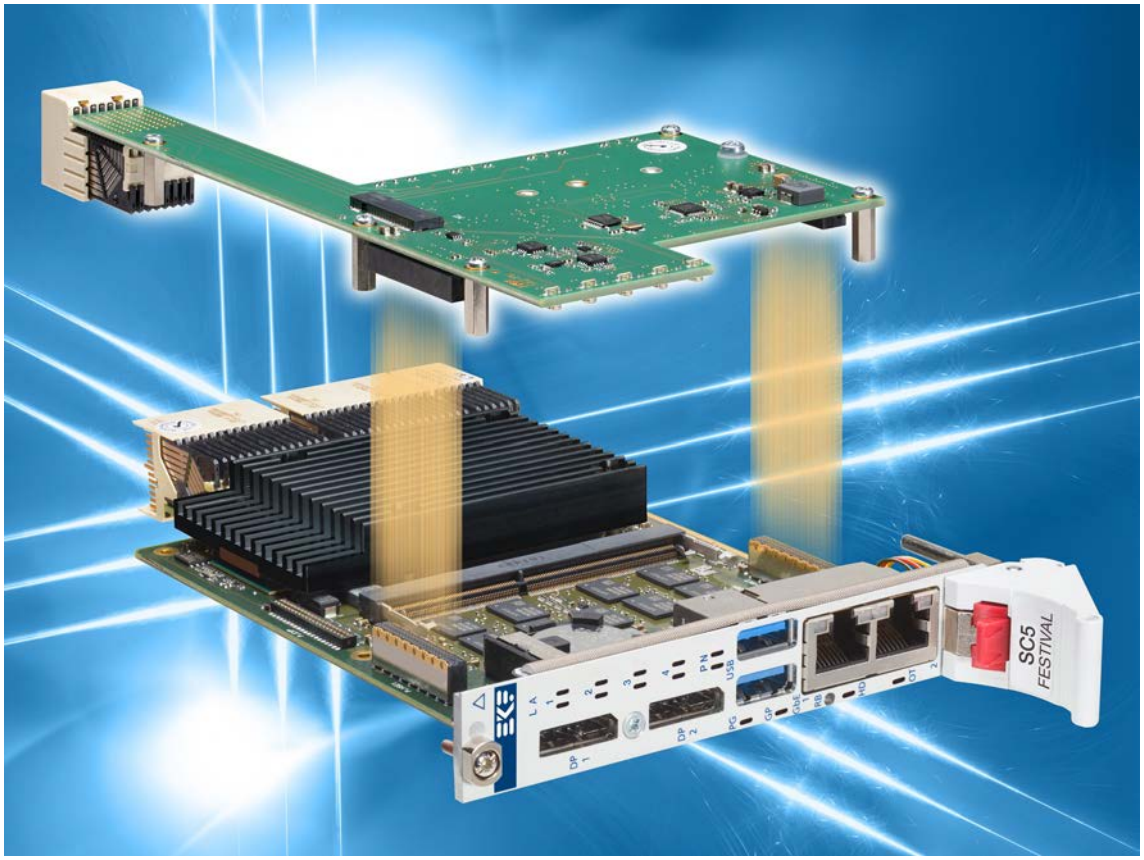


SC5-FESTIVAL with S80-P6 Mezzanine

SC5-FESTIVAL w. S80-P6 Low Profile Mezzanine

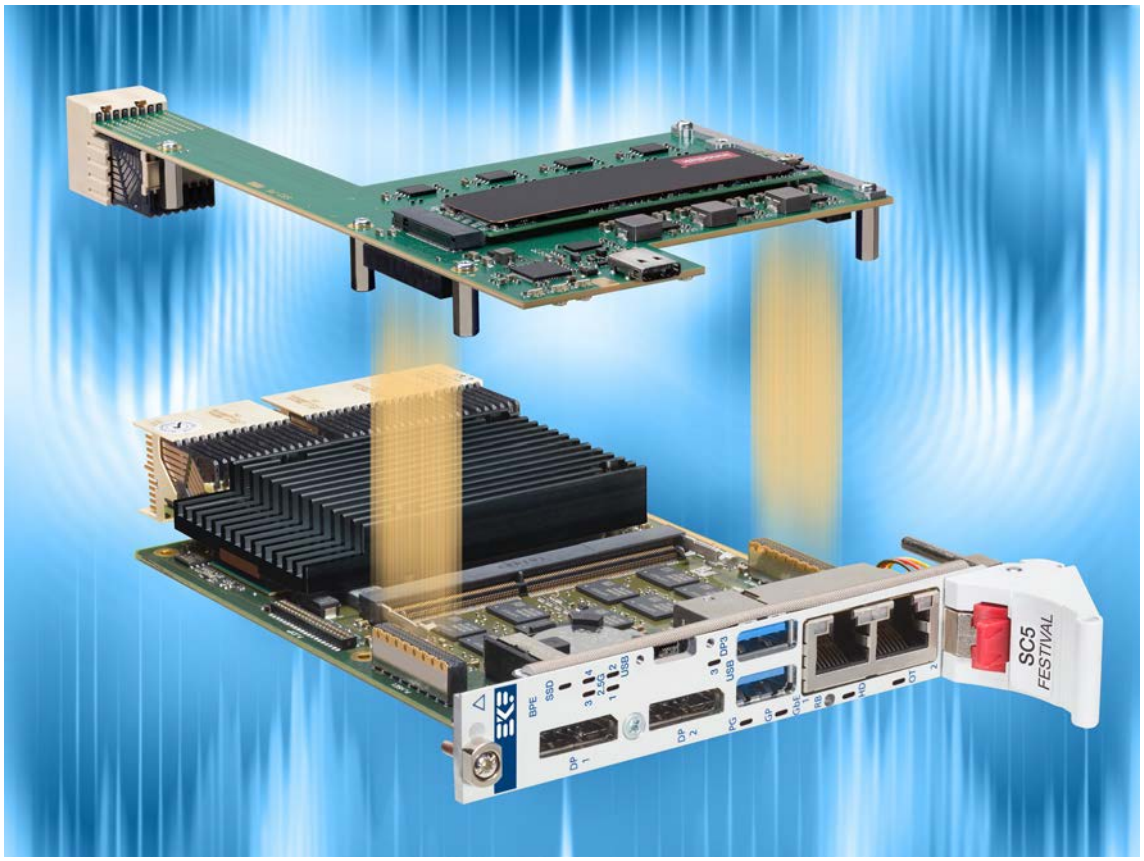


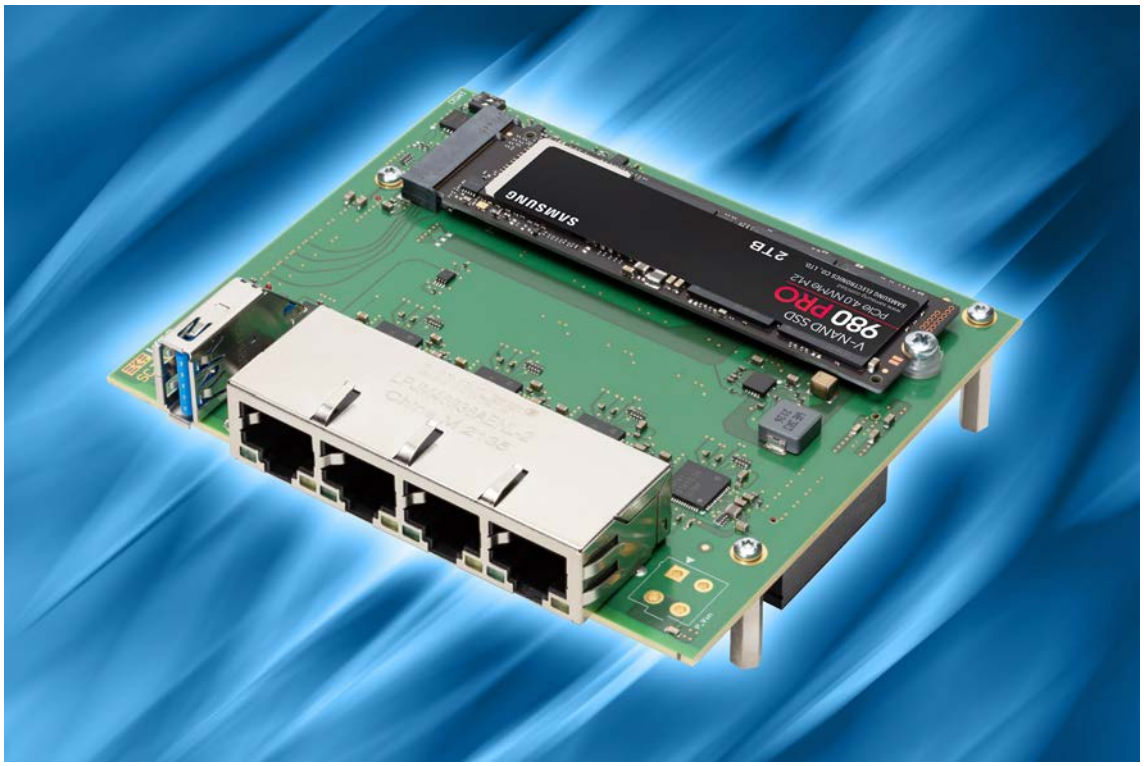
S82-P6



SC5-FESTIVAL w. S82-P6 Low Profile Mezzanine

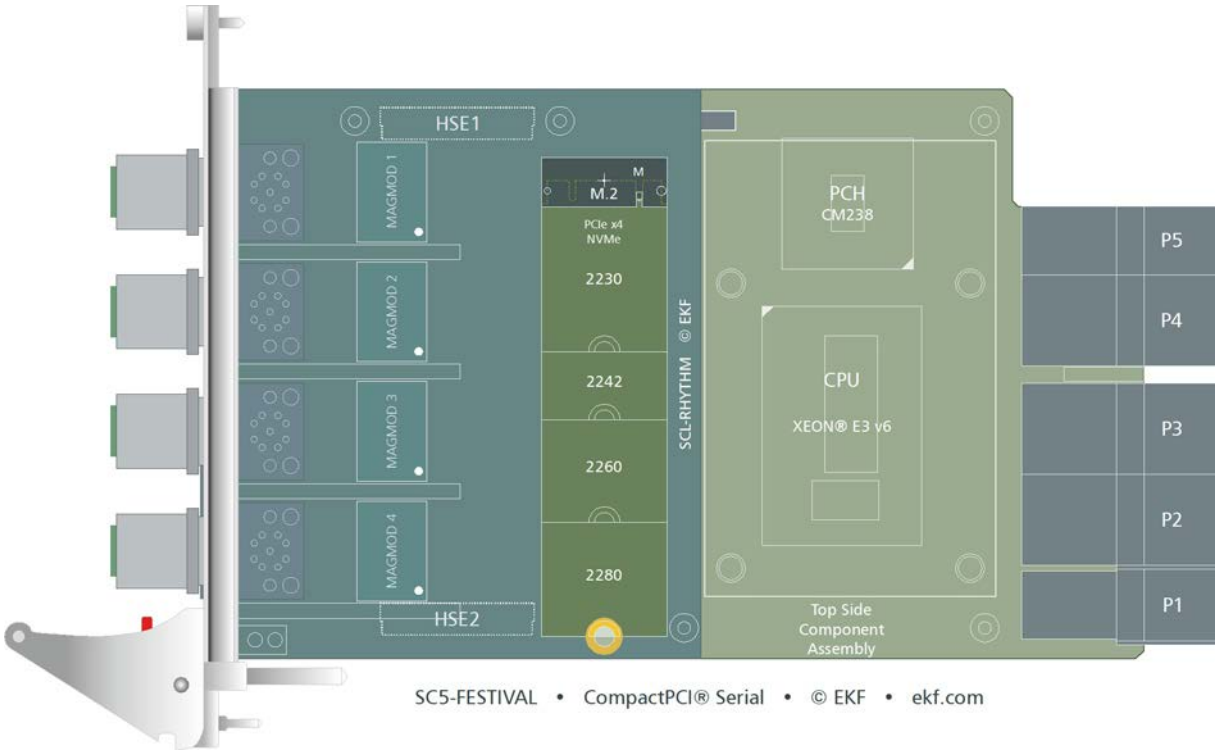
SC5-FESTIVAL w. S83-P6





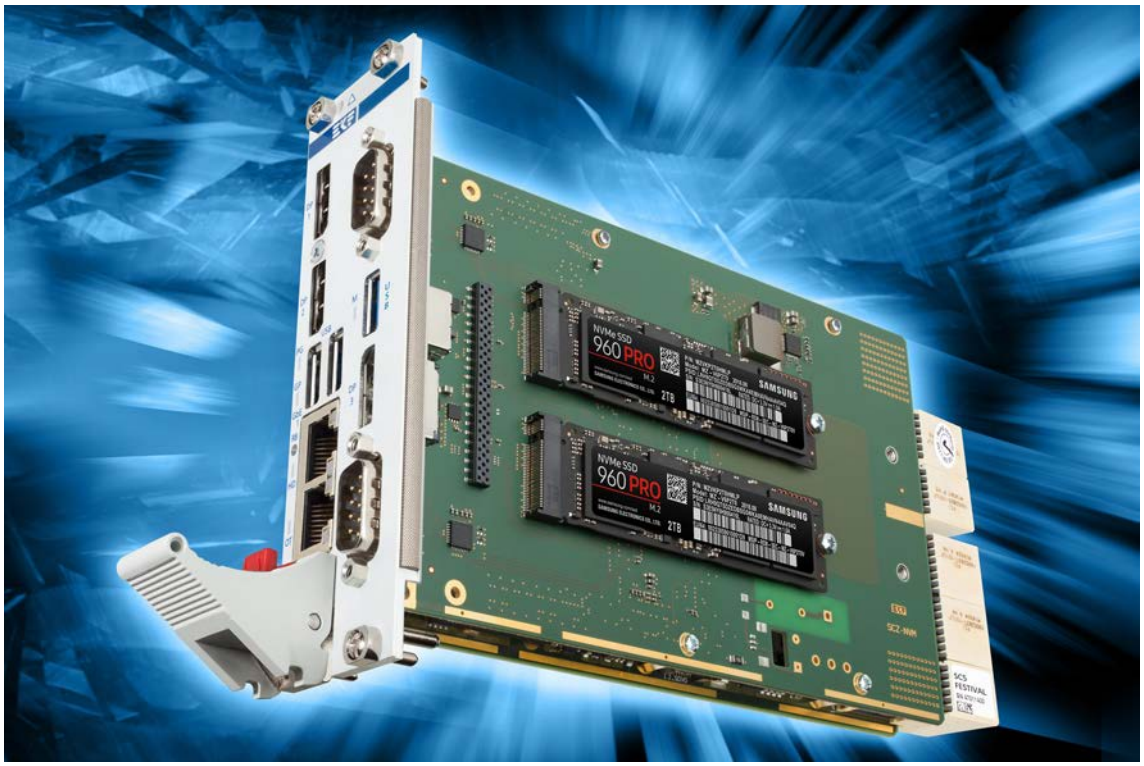
SCJ-VEENA • Quad 2.5GBASE-T NICs

8HP Assembly w. SCJ-VEENA



SC5-FESTIVAL w. SCL-RHYTHM Side Card (8HP Assembly)

SCZ-NVM Side Card (8HP/12HP Assembly)



SC5-FESTIVAL w. SCZ-NVM Side Card (8HP Assembly)

8HP Assembly SC5-FESTIVAL w. PCU-P400-UPTEMPO Side Card

8HP Assembly w. PCU-P400-UPTEMPO

8HP Assembly w. PCU-P400-UPTEMPO

Mezzanine Connectors Related Documents
www.ekf.com/s/sc4/new_mezzanine_connectors.pdf

P-EXP	
I/F Type	Controller
LPC (Low Pin Count)	PCH
HD Audio	PCH
I^2C	PCH (I^2C[0])
2 x UART (TTL)	PCH

P-HSE1	
I/F Type	Controller
4 x PCIe Gen3 or 4 x SATA 6G	PCH
2 x USB 2.0, 1 x USB 3.0	PCH

P-HSE2	
I/F Type	Controller
4 x PCIe Gen3	PCH
1 x DisplayPort	PCH
I^2C	PCH (I^2C[0])

CompactPCI® Serial

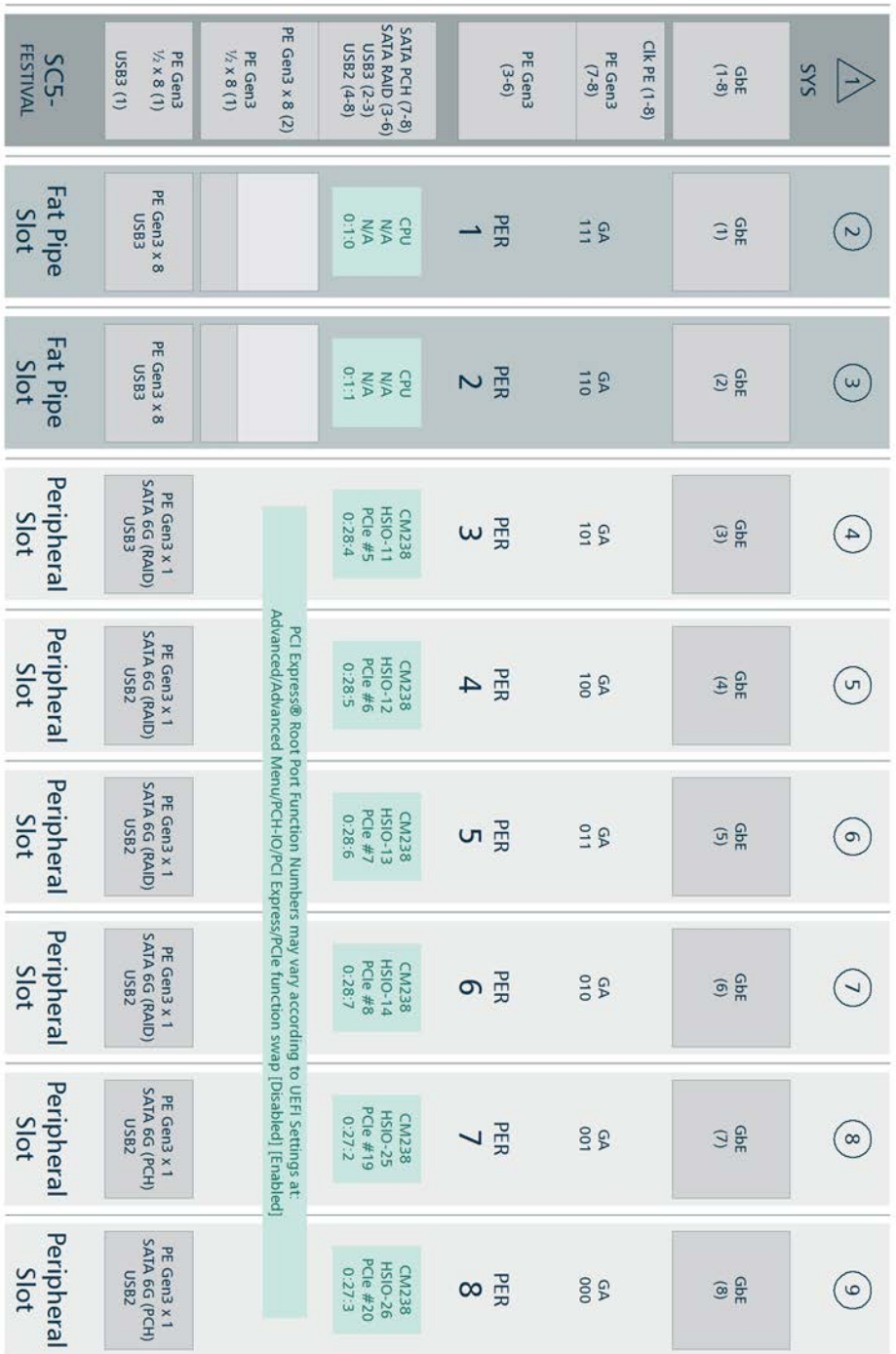
System Slot Controller

The PICMG® CompactPCI® Serial specification defines a card slot system based on the high speed data links PCI Express®, SATA, Ethernet and USB. The SC5-FESTIVAL, designed to act as a CompactPCI® Serial system slot controller, provides the resources of these interfaces. The backplane distributes them in the form of point to point connections to the peripheral slots.

The SC5-FESTIVAL provides most communication channels defined by CompactPCI® Serial on the backplane:

- Two PCIe links x8, 2.5GT/s, 5GT/s or 8GT/s (Fat Pipes)
- Six PCIe links x1, 2.5GT/s, 5GT/s or 8GT/s
- Six SATA ports (6G)
- Three USB 3.0 ports
- Five USB 2.0 ports
- Eight Gigabit Ethernet ports (requires S80-P6 low profile mezzanine module)

These resources will be distributed on a typical 9-slot (5-slot) CompactPCI® Serial backplane as follows:

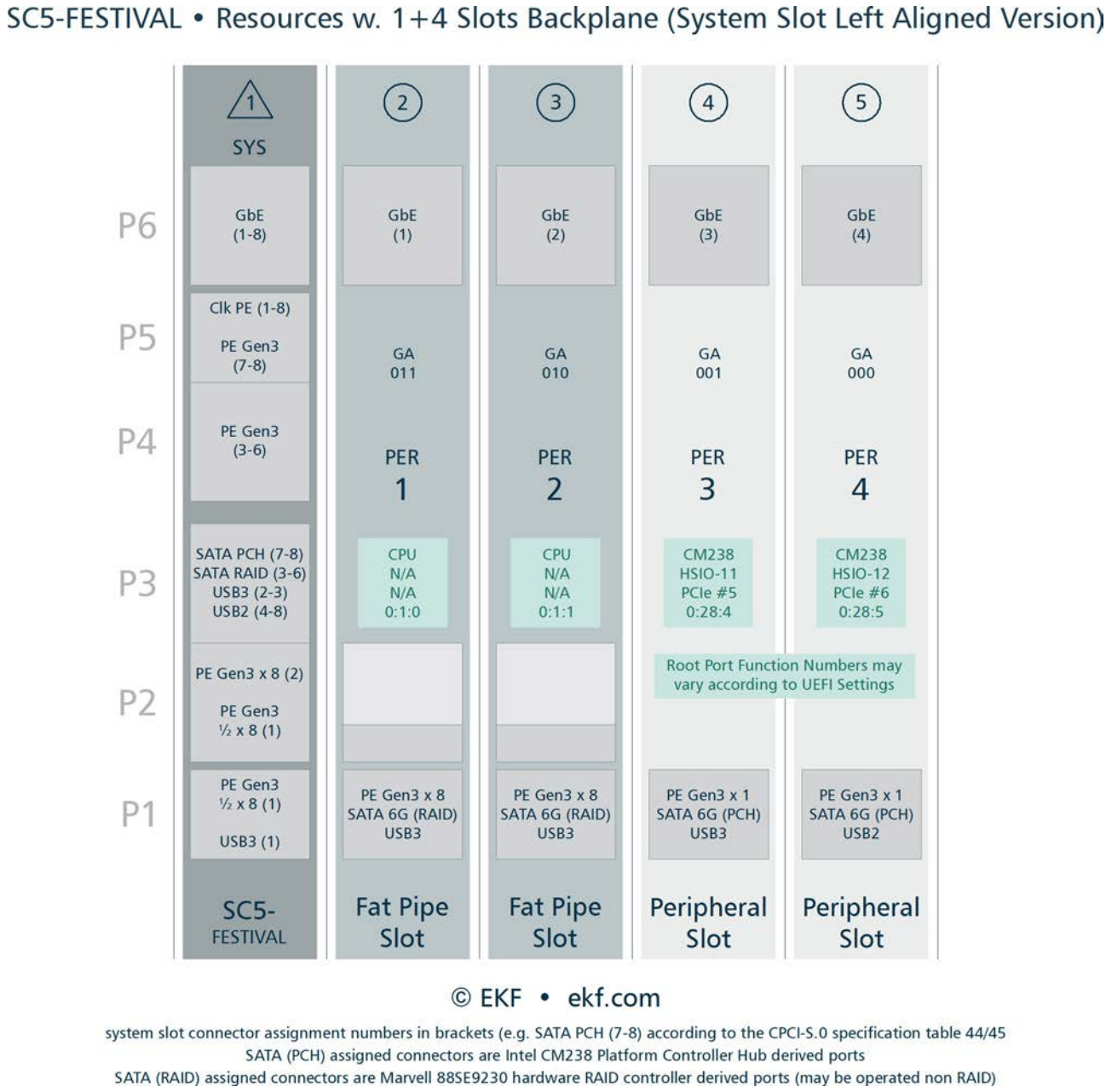


Backplane Resources SC5-FESTIVAL (System Slot Left Aligned)

www.ekf.com/s/sc5/img/sc5_backplane.pdf

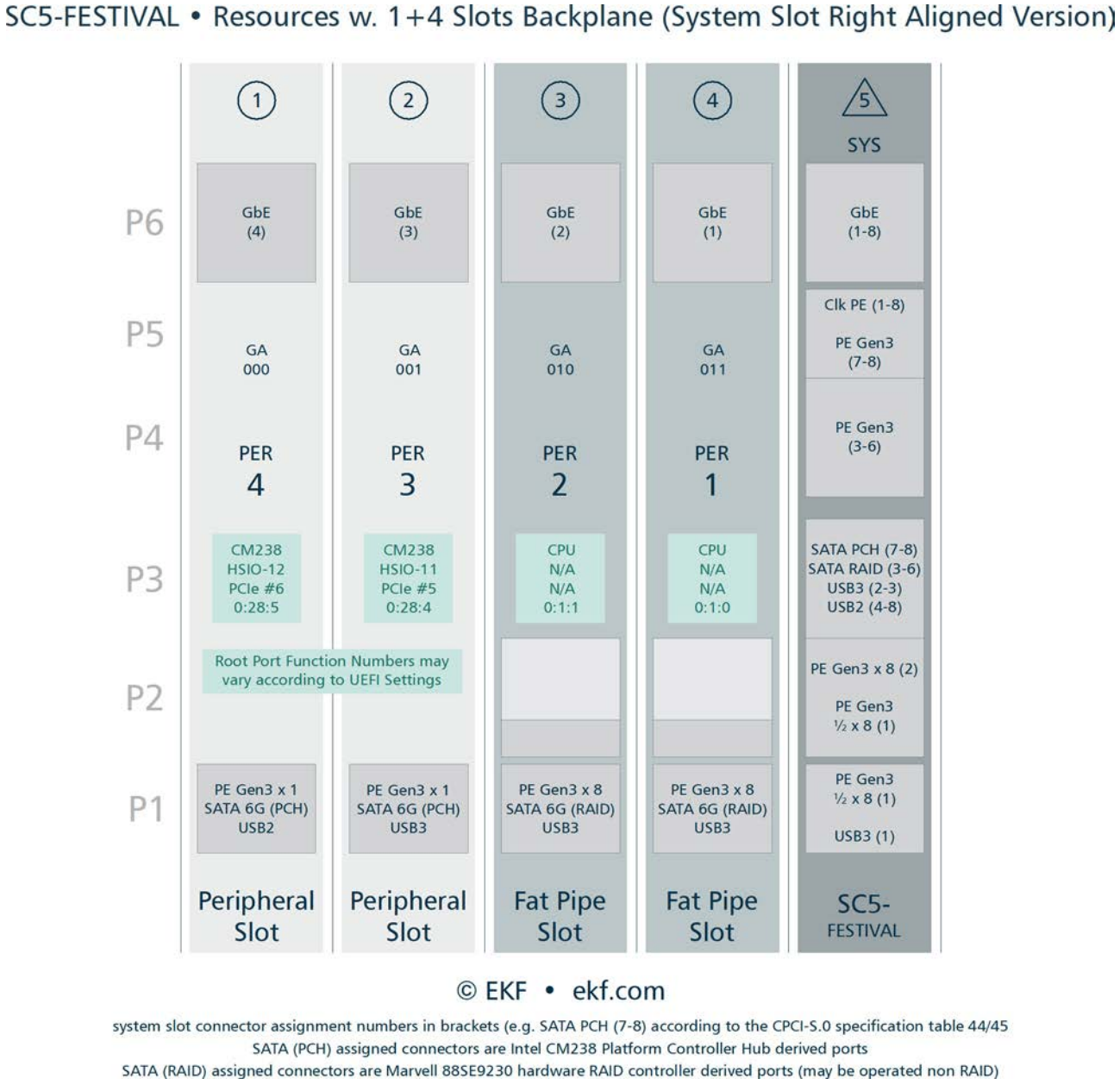
Backplane Resources SC5-FESTIVAL (System Slot Right Aligned)

www.ekf.com/s/sc5/img/sc5_backplane.pdf



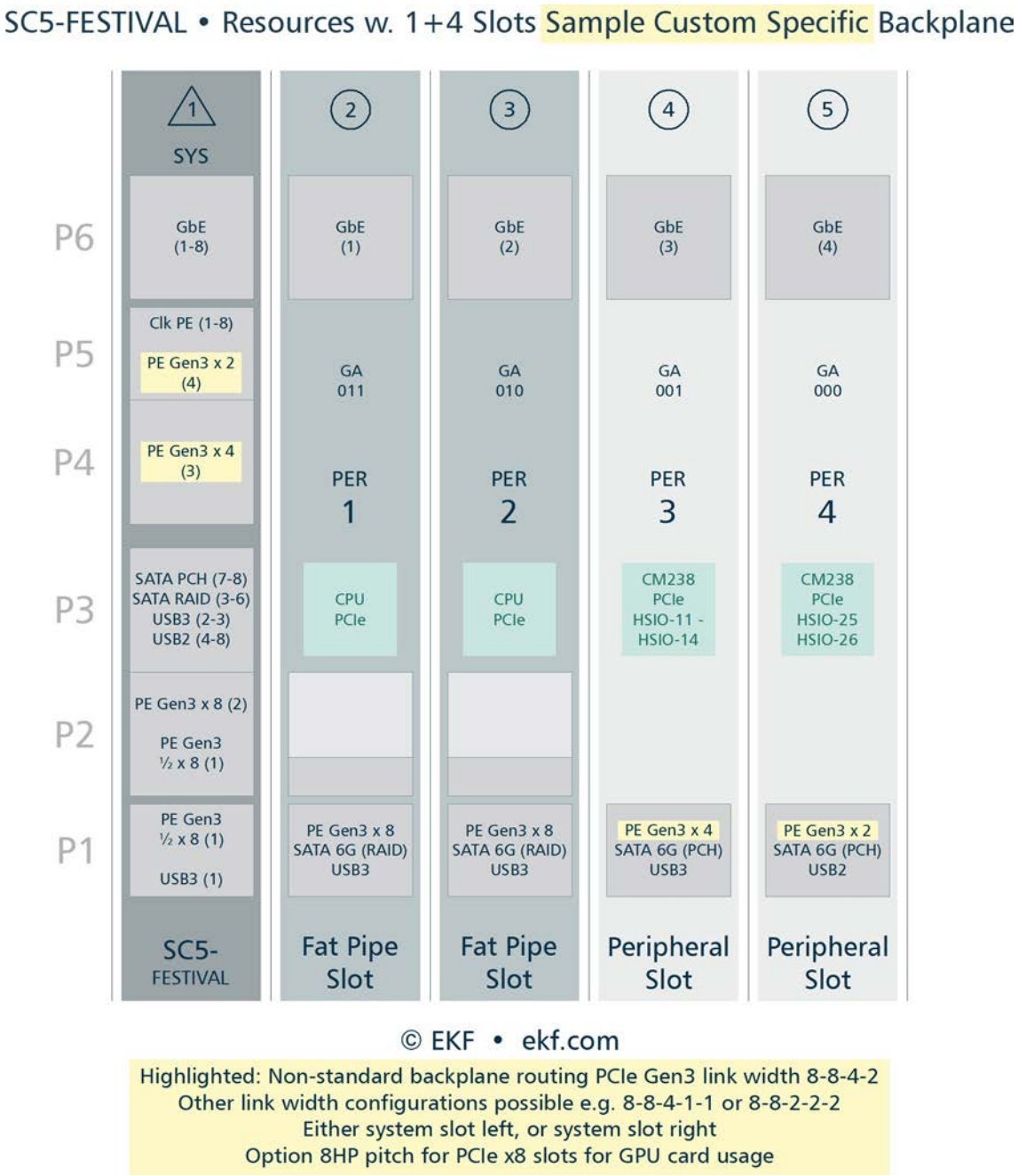
Backplane Resources w. 1-4 Slots Backplane

www.ekf.com/s/sc5/img/sc5_backplane.pdf



Backplane Resources w. 1-4 Slots Backplane

www.ekf.com/s/sc5/img/sc5_backplane.pdf



Sample Custom Backplane for Optimum PCIe Usage

www.ekf.com/s/sc5/img/sc5_backplane.pdf

PCIe link width (PCH) configurable via recent (2020) UEFI/BIOS & ME:
Setup (F2): Advanced -> PCI Configuration -> PCH PCI Express Configuration -> Select Link Width of PCH PCIe Controller 1-5

Peripheral Slot Operation

Beyond the typical role as system slot card, the SC5-FESTIVAL is operable in periphery slots as well. In this case it acts as a satellite system, linked to other (processor-) boards by its backplane Ethernet connections. The other resources associated with the backplane like PCI Express, SATA or USB are not usable in this situation.

Some of the following, system slot dedicated control signals get an altered function or will be disconnected from the backplane:

- PWRBTN# (Connector P1 Pin C3) will be disconnected
- PWR_FAIL# (Connector P1 Pin F3) becomes GA1
- PRST# (Connector P1 Pin H2) becomes RST# and may be disconnected
- WAKE# (Connector P1 Pin I2) will be disconnected
- SGPIO (Connector P1 Pins G3/H3/J3/K3) will be disconnected

One result of that is, that a SC5-FESTIVAL plugged into a peripheral slot will not get a reset even if the system controller forces the reset signal on the backplane to an active state.

Board Hot-Plug

Hot-plug of the SC5-FESTIVAL is not supported, no matter whether it is working as a system controller or satellite board. But it is possible for the SC5-FESTIVAL to detect and handle hot-plug events of periphery boards. This feature is supported on all interfaces fed to the CompactPCI Serial backplane, i.e.

- PCI Express 3.0
- SATA 3.0
- USB 2.0/3.0
- Gigabit Ethernet

Except of PCI Express hot-plug is enabled on all interfaces by default. For PCI Express the UEFI/BIOS (Build #138 or later) setup of the SC5-FESTIVAL provides settings to switch on or off the hot-plug feature, for Fat Pipe or Standard peripheral slots on different menu places:

- After Power-On press function key <F2> to enter setup menu
- Fat Pipe Slots:
  Advanced→Advanced Menu→PCI Configuration→SA PCI Express Configuration→Hot-Plug
- Standard Slots:
  Advanced→Advanced Menu→PCI Configuration→PCH PCI Express Configuration
  PCH PCIe Root Port [5-8/19/20]→Hot-Plug

Supplementary Information

Useful Information Related to CompactPCI® Serial	
CompactPCI® Serial Concise Overview	www.ekf.com/s/serial_concise.pdf
CompactPCI® Serial All You Need to Know	www.ekf.com/s/smart_solution.pdf

3D Clamshell Available for Cooling & Rugged Environments

Installing and Replacing Components

Before You Begin

Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for repair.

Installing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system

- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related CompactPCI® slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

Removing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Identify the board, be sure to touch the board only at the front panel
- Unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.

EMC Recommendations

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Replacement of the Battery

When your system is turned off, a battery maintains the voltage to run the time-of-day clock. The battery should last during the lifetime of the SC5-FESTIVAL.

However, some versions of SC5-FESTIVAL are delivered with a battery holder which makes it possible for the user to replace the coin cell. Use a CR2032 cell as replacement part to ensure an extended temperature range. Be careful when removing the old cell and inserting the new one.

For boards with a soldered battery the old battery must be desoldered, and the new one soldered. We suggest that you send back the board to EKF for battery replacement.

Warning

Danger of explosion if the battery is incorrectly replaced or shorted. Replace only with the same or equivalent type. Do not expose a battery to fire.

Technical Reference

Local PCI Devices

The following table shows the on-board PCI devices and their location within the PCI configuration space. Several devices are part of the processor and platform controller hub CM238.

Bus #	Device #	Function #	Vendor ID	Device ID	Description
0	0	0	0x8086	0x5918	Processor Host Bridge/DRAM Controller
0	1	0	0x8086	0x1901	Processor PCI Express Controller (→ x8 CPCI-S.0)
0	1	1	0x8086	0x1905	Processor PCI Express Controller (→ x8 CPCI-S.0)
0	2	0	0x8086	0x591D	Processor Integrated Graphics Device
0	8	0	0x8086	0x1911	Gaussian Mixture Model Device
0	20	0	0x8086	0xA12F	USB 3.0 xHCI Controller
0	20	2	0x8086	0xA131	Thermal Subsystem
0	21	0-1	0x8086	0xA160-A161	I^2C Controller #0-1
0	22	0-1	0x8086	0xA13A-A13B	Intel ME Interface #1-2
0	22	2	0x8086	0xA13C	Intel ME IDE Redirection
0	22	3	0x8086	0xA13D	Intel ME Keyboard Text Redirection
0	22	4	0x8086	0xA13E	Intel ME Interface #3
0	23	0	0x8086	0xA102 0xA106	SATA: AHCI Mode [1] SATA: RAID Capable [2]
0	27	0-1	0x8086	0xA169-A16A	PCH PCI Express Root Port #19-20 (→ CPCI-S.0)
0	28	0	0x8086	0xA110	PCH PCI Express Port #1 (→ x2 Marvell 88SE9230)
0	28	2	0x8086	0xA112	PCH PCI Express Port #3 (→ Intel i210IT)
0	28	4-7	0x8086	0xA114-A117	PCH PCI Express Port #5-8 (→ CPCI-S.0)
0	29	0-3	0x8086	0xA118-A11B	PCH PCI Express Port #9-12 (→ HSE2)
0	29	4	0x8086	0xA11C	PCH PCI Express Port #13 (→ x4 HSE1)
0	30	0-1	0x8086	0xA127-A128	UART Controller #0-1
0	31	0	0x8086	0xA154	LPC Bridge
0	31	3	0x8086	0xA170	Intel High Definition Audio
0	31	4	0x8086	0xA123	SMBus Controller
0	31	5	0x8086	0xA124	SPI Controller
0	31	6	0x8086	0x15B7	Ethernet Controller NC1 (Intel i219LM)
1 [3]	00	0	0x1B4B	0x9230	SATA Host Controller (Marvell 88SE9230)
2 [3]	00	0	0x8086	0x157B	Ethernet Controller NC2 (Intel i210IT)

1) Depends on UEFI/BIOS settings.

2) Depending on UEFI/BIOS settings different RAID modes may lead to other Device IDs.

3) Bus number can vary depending on the PCI enumeration schema implemented in UEFI/BIOS.

Local SMB/I²C Devices

The SC5-FESTIVAL contains devices that are attached to the System Management Bus (SMBus). These are the SPD EEPROMs for the on-board memory or the possibly plugged SODIMM, a general purpose serial EEPROM containing board configuration data, the supply voltage/temperature controlling device NCT7491, a set of board control and status registers as well as two general purpose, non-volatile electronic jumpers. Additional devices may be connected to the different I²C controllers of the CM238 via the CompactPCI® Serial backplane signals I²C_SCL (P1 B2) and I²C_SDA (P1 C2) or the mezzanine expansion connectors P-HSE2 or P-EXP.

Controller	Address	Description
SMBus	0x2C	Hardware Monitor/Memory Down Temperature Sensor (7491)
SMBus	0x2E	Board Control/Status
SMBus	0x2F	Non-volatile Electronic Jumper
SMBus	0x50 0x36/0x37	SPD EEPROM of On-board Memory 4KBit EEPROM Select Bank 0/1
SMBus	0x52 0x36/0x37	SPD EEPROM of SODIMM 4KBit EEPROM Select Bank 0/1
SMBus	0x57	General Purpose EEPROM 2KBit
I2C[0]	[1)]	P-HSE2 (Pins A22/A23), P-EXP (Pins 29/30)
I2C[1]	[1)]	Serial Backplane Connector P1 (Pins B2/C2)

[1)] Address depends on devices attached

Hardware Monitor NCT7491

Attached to the SMBus, the SC5-FESTIVAL is provided with the hardware monitor NCT7491. This device is capable to observe the temperatures of the board, processor cores, and on-board memory, as well as several supply voltage rails with a resolution of 10 bit. The following table shows the mapping of the voltage inputs of the NCT7491 to the corresponding supply voltages of the SC5-FESTIVAL:

Input	Source	Resolution	Register (MSB/LSB)
VCCP	Processor Core Voltage	2.93mV	0x21/0x76[3:2]
VTT	+1.0V	2.20mV	0x1E/0x1F[5:4]
+2.5V/THERM#	+1.2V	3.26mV	0x20/0x76[1:0]
VCC	+3.3V	4.29mV	0x22/0x76[5:4]
+5Vin	+5V	6.54mV	0x23/0x76[7:6]
+12Vin	+12V	15.92mV	0x24/0x77[1:0]
PECI	Core #0 absolute Temperature	1°C	0x04
PECI	Core #1 absolute Temperature	1°C	0x05
PECI	Core #2 absolute Temperature	1°C	0x06
PECI	Core #3 absolute Temperature	1°C	0x07
D1+/D1-	Memory Down absolute Temperature	0.25°C	0x25/0x77[3:2]
Local TEMP	SC5 Surface Temperature	0.25°C	0x26/0x77[5:4]

Beside the continuous measuring of temperatures and voltages the NCT7491 may compare these values against programmable upper and lower boundaries. As soon as a measurement violates the allowed value range, the NCT7491 can request an over-temperature event on GPP_D1 input of the CM238 or an interrupt via the GPP_D2 input (which may result in a system management interrupt).

Board Control and Status Registers (BCSR)

A set of board control and status registers allow to program special features on the SC5-FESTIVAL:

- Assert a full reset
- Control activity of front panel reset and power event button
- Program time-outs and trigger a watchdog
- Get access to two LEDs in the front panel
- Get power fail and watchdog status of last board reset

The register set consists of five registers located on the SMBus at Device ID=0x5c on the following addresses:

- 0xA0: CMD_CTRL0_WR: Write to Control Register 0 (Write-Only)
- 0xA1: CMD_CTRL0_RD: Read from Control Register 0 (Read-Only)
- 0xB0: CMD_STAT0_WR: Write to Status Register 0 (Write-Clear)
- 0xB1: CMD_STAT0_RD: Read from Status Register 0 (Read-Only)
- 0xB2: CMD_STAT1_WR: Write to Status Register 1 (Write-Clear)
- 0xB3: CMD_STAT1_RD: Read from Status Register 1 (Read-Only)
- 0xC1: CMD_PLDREV_RD: Read from PLD Revision Register (Read-Only)

To prevent misfunction accesses to the registers should be done by SMBus “Byte Data” commands. Further writes to read-only or reads to write-only registers should be omitted.

Write/Read Control Register 0

Write: SMBus Address 0xA0 Default after reset: 0x00
Read: SMBus Address 0xA1

Bit	Description CMD_CTRL0
7	GPLED 0=Green part of the front panel LED GP is off (Default) 1=Green part of the front panel LED GP is on
6	FPDIS 0=Enable the front panel handle switch (Default) 1=Disable the front panel handle switch
5	FERP# 0=The front panel handle switch generates a power event (Default) 1=The front panel handle switch generates a system reset
4:3	WDGT0:WDGT1 Maximum Watchdog retrigger time: 0:0 2 sec 1:0 10 sec 0:1 50 sec 1:1 250 sec
2	WDGTRG Retrigger Watchdog. Any change of this bit will retrigger the watchdog. After a system reset the watchdog is in an inactive state. The watchdog is armed on the 1st edge of this bit.
1	PGLED 0=Red part of the front panel LED PG is off (Default) 1=Red part of the front panel LED PG is blinking
0	SRES 0=Normal operation (Default) 1=A full system reset is performed

Read/Clear Status Register 0

Write: SMBus Address 0xB0
Read: SMBus Address 0xB1

Bit	Description CMD_STAT0
7	PF18S 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.8S voltage regulator
6	PF10S 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.0S voltage regulator
5	PF10A 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.0A voltage regulator
4	PF25S4 0=Normal operation 1=Last system reset may be caused by a power failure of the +V2.5S4 voltage regulator
3	PF12S4 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.2S4 voltage regulator
2	PFVRST 0=Normal operation 1=Last system reset may be caused by a power failure of the +VCCST load switch
1	PFVRIO 0=Normal operation 1=Last system reset may be caused by a power failure of the +VCCIO voltage regulator
0	PFVRC 0=Normal operation 1=Last system reset may be caused by a power failure of the IMVP-8 voltage regulator

The bits in this register are sticky, i.e. their state will be kept even if a system reset occurs. To clear the bits a write to the register with arbitrary data may be performed.

Read/Clear Status Register 1

Write: SMBus Address 0xB2
Read: SMBus Address 0xB3

Bit	Description CMD_STAT1
7	WDGARMD 0=Normal operation 1=The watchdog is armed and has to be retriggered within its time-out period
6	WDGRST 0=Normal operation 1=Last system reset may be caused by a watchdog time-out
5	WDGHT 0=Normal operation 1=The watchdog already has elapsed half of its time-out period
4	PF5PS 0=Normal operation 1=Last system reset may be caused by a power failure of the +V5PS voltage regulator
3	PF5S 0=Normal operation 1=Last system reset may be caused by a power failure of the +V5S voltage regulator
2	PF33L 0=Normal operation 1=Last system reset may be caused by a power failure of the +V3.3LAN load switch
1	PF33A 0=Normal operation 1=Last system reset may be caused by a power failure of the +V3.3A voltage regulator
0	PF33S 0=Normal operation 1=Last system reset may be caused by a power failure of the +V3.3S voltage regulator

Except of WDGHT and WDGARMD the bits in this register are sticky, i.e. their state will be kept even if a system reset occurs. To clear the bits a write to the register with arbitrary data may be performed.

Read PLD Revision Register

Write: Not allowed
Read: SMBus Address 0xC1

Bit	Description CMD_PLDREV
7:0	PLDREV Read PLD Revison Number

GPIO Usage

GPIO Usage CM238 PCH

GPIO Usage CM238 PCH				
GPIO	USAGE	DIR	Function	Description
Group A (GPP_A)				
A0	Native	IN	RCIN#	Keyboard Reset, to P-EXP Pin 13
A1-A4	Native	I/O	LPC_AD[0-3]	LPC Address/Data Lines
A5	Native	OUT	LPC_FRAME#	LPC Frame
A6	Native	IN	SERIRQ	Serialized IRQ
A7	Native	IN	PIRQA#	Not used on SC5 (pulled via resistor to +3.3V)
A8	Native	IN	CLKRUN#	Not used on SC5 (pulled via resistor to +3.3V)
A9	Native	OUT	CLKOUT_LPC0	24MHz LPC Clock, to P-EXP Pin 3
A10	Native	OUT	CLKOUT_LPC1	24MHz LPC Clock, to TPM
A11	Native	IN	PME#	Power Management Event, to P-EXP Pin 14
A12-A13	GPIO	IN	N/A	Not connected on SC5
A14	Native	OUT	N/A	Not connected on SC5
A15-A16	GPIO	IN	N/A	Not connected on SC5
A17-A19	GPIO	IN	HW_REV[0:2]	PCB Revision Code HW_REV[2:0] GPIO[19:17] 000 001 010 ... 110 111 Revision 0 1 2 6 7
A20	GPIO	OUT	SE_SYS_WP	TPM2.0 Physical Present Pin
A21-A23	GPIO	IN	N/A	Not connected on SC5
Group B (GPP_B)				
B0	GPIO	OUT	ENABLE_NC2	Enable Ethernet Controller NC2
B1-B5	GPIO	IN	N/A	Not connected on SC5
B6	Native	IN	CLKREQ1#	CompactPCI® Clock Request Slot 1 (P5 C5: 1_PE_CLKE#)
B7	Native	IN	CLKREQ2#	CompactPCI® Clock Request Slot 2 (P5 F5: 2_PE_CLKE#)
B8	Native	IN	CLKREQ3#	CompactPCI® Clock Request Slot 3 (P5 I5: 3_PE_CLKE#)
B9	Native	IN	CLKREQ4#	CompactPCI® Clock Request Slot 4 (P5 L5: 4_PE_CLKE#)
B10	Native	IN	CLKREQ5#	CompactPCI® Clock Request Slot 5 (P5 A6: 5_PE_CLKE#)
B11-B12	GPIO	IN	N/A	Not connected on SC5
B13	Native	OUT	PLTRST#	Platform Reset
B14	Native	OUT	SPEAKER	Speaker, to P-EXP Pin 39

GPIO Usage CM238 PCH				
GPIO	USAGE	DIR	Function	Description
B15-B17	GPIO	IN	N/A	Not connected on SC5
B18	GPIO	OUT	N/A	Not used on SC5, Hardware Strap to disable TCO Watchdog
B19-B21	GPIO	IN	N/A	Not connected on SC5
B22	GPIO	OUT	USB_POWEN1	USB Front Panel Right Port Power Enable
B23	GPIO	OUT	USB_POWEN2	USB Front Panel Left Port Power Enable
Group C (GPP_C)				
C0	Native	I/O	SMBCLK	SMBus Clock Line
C1	Native	I/O	SMBDATA	SMBus Data Line
C2	GPIO	IN	N/A	Not used on SC5, pulled to +3.3V
C3	Native	I/O	SML0CLK	SMLink[0] Clock Line, to Ethernet Controller NC1
C4	Native	I/O	SML0DATA	SMLink[0] Data Line, to Ethernet Controller NC1
C5	GPIO	OUT	N/A	Not connected on SC5
C6-C7	GPIO	IN	N/A	Not connected on SC5
C8	Native	IN	UART0_RXD	UART[1] RXD Line, to P-EXP Pin 25
C9	Native	OUT	UART0_TXD	UART[1] TXD Line, to P-EXP Pin 23
C10	Native	OUT	UART0_RTS#	UART[1] RTS# Line, to P-EXP Pin 24
C11	Native	IN	UART0_CTS#	UART[1] CTS# Line, to P-EXP Pin 26
C12	Native	IN	UART1_RXD	UART[2] RXD Line, to P-EXP Pin 18
C13	Native	OUT	UART1_TXD	UART[2] TXD Line, to P-EXP Pin 17
C14	Native	OUT	UART1_RTS#	UART[2] RTS# Line, to P-EXP Pin 20
C15	Native	IN	UART1_CTS#	UART[2] CTS# Line, to P-EXP Pin 27
C16	Native	I/O	I2C0_DATA	I^2C Data Line, to Connectors P-HSE2 Pin A23/P-EXP Pin 30
C17	Native	I/O	I2C0_CLK	I^2C Clock Line, to Connectors P-HSE2 Pin A22/P-EXP Pin 29
C18	Native	I/O	I2C1_DATA	I^2C Data Line, to CompactPCI Serial P1 Pin C2
C19	Native	I/O	I2C1_CLK	I^2C Clock Line, to CompactPCI Serial P1 Pin B2
C20-C23	GPIO	IN	N/A	Not connected on SC5

GPIO Usage CM238 PCH				
GPIO	USAGE	DIR	Function	Description
Group D (GPP_D)				
D0	GPIO	IN	CPCI_PWR_FAIL#	Sense CompactPCI Serial Power Failure, P1 Pin F3
D1	GPIO	IN	PM_MEMTS#	Memory Thermal Sensor Event
D2	GPIO	IN	HM_INT#	Hardware Monitor NCT7491 Alert Line
D3-D8	GPIO	IN	N/A	Not connected on SC5
D9	GPIO	IN	GP_JUMP#	Reset UEFI/BIOS Setup to Factory Defaults, Jumper J-GP
D10	GPIO	IN	CPCI_SYSEN#	Sense CompactPCI Serial System Slot Enable, P1 Pin L2
D11	GPIO	OUT	GP_LED_RED	General Purpose Red LED Control (via PLD)
D12-D20	GPIO	IN	N/A	Not connected on SC5
D21	GPIO	OUT	SE_SYS_WP	General Purpose Serial EEPROM Write Protection
D22	GPIO	OUT	PPSM_EN	Connect IEEE 1588 PPS/PPM to J-GP and CompactPCI Serial P1 LO: Isolate PPS/PPM Signals HI: Connect PPS/PPM to J-GP/P1
D23	GPIO	IN	N/A	Not connected on SC5
Group E (GPP_E)				
E0	Native	IN	SATA#PCIE12	P-HSE1 HS Lanes 1/2 Configuration LO: Configured as SATA HI: Configured as PCIe
E1	Native	IN	SATA#PCIE12	Shorted to GPP_E0
E2	Native	IN	SATA#PCIE34	P-HSE1 HS Lanes 3/4 Configuration LO: Configured as SATA HI: Configured as PCIe
E3-E7	GPIO	IN	N/A	Not connected on SC5
E8	Native	OUT	SATALED#	Signal PCH SATA activity via green HD LED in Front Panel (to PLD)
E9	Native	IN	USB_FP_OC1#	USB Front Panel Right Port Overcurrent Detect
E10	Native	IN	USB_FP_OC2#	USB Front Panel Left Port Overcurrent Detect
E11	Native	IN	USB_HSE1_OC#	Overcurrent Detect on any P-HSE1 USB Port
E12	GPIO	IN	N/A	Not connected on SC5

GPIO Usage CM238 PCH				
GPIO	USAGE	DIR	Function	Description
Group F (GPP_F)				
F0	Native	IN	SATA#PCIE34	Shorted to GPP_E2
F1-F9	GPIO	IN	N/A	Not connected on SC5
F10	Native	OUT	SGPIO_CLOCK	CompactPCI Serial GPIO Bus CLOCK (P1 J3: SATA_SCL)
F11	Native	OUT	SGPIO_LOAD	CompactPCI Serial GPIO Bus LOAD (P1 K3: SATA_SL)
F12	GPIO	IN	SGPIO_IN	CompactPCI Serial GPIO Bus DATAIN (P1 G3: SATA_SDI)
F13	Native	OUT	SGPIO_OUT	CompactPCI Serial GPIO Bus DATAOUT (P1 H3: SATA_SDO)
F14-F23	GPIO	IN	N/A	Not connected on SC5
Group G (GPP_G)				
G0-G18	GPIO	IN	N/A	Not connected on SC5
G19	Native	IN	SMI#	Connected to P-EXP SMI# Signal (Pin 15)
G20-G23	GPIO	IN	BOARD_CFG	Board Configuration Jumpers BOARD_CFG[0:3]
Group H (GPP_H)				
H0	Native	IN	PCIE_CLK_REQ6#	CompactPCI® Clock Request Slot 6 (P5 D6: 6_PE_CLKE#)
H1	Native	IN	PCIE_CLK_REQ7#	CompactPCI® Clock Request Slot 7 (P5 G6: 7_PE_CLKE#)
H2	Native	IN	PCIE_CLK_REQ8#	CompactPCI® Clock Request Slot 8 (P5 J6: 8_PE_CLKE#)
H3	Native	IN	PCIE_CLK_REQ9#	Ethernet Controller NC1 Clock Request
H4-H11	GPIO	IN	N/A	Not connected on SC5
H12	GPIO	OUT	N/A	Not connected on SC5
H13-H23	GPIO	IN	N/A	Not connected on SC5
Group I (GPP_I)				
I0	Native	IN	DDPB_HPD1	DisplayPort Front Panel Upper Port Hot Plug Detect
I1	Native	IN	DDPB_HPD2	DisplayPort Front Panel Lower Port Hot Plug Detect
I2	Native	IN	DDPB_HPD3	DisplayPort P-HSE2 Port Hot Plug Detect
I3	GPIO	IN	N/A	Not connected on SC5
I4	GPIO	IN	N/A	Not used on SC5 (pulled via resistor to GND)
I5	Native	OUT	DDPB_CTRLCLK	DisplayPort Front Panel Upper Port DDC_CLK
I6	Native	I/O	DDPB_CTRLDTA	DisplayPort Front Panel Upper Port DDC_DATA
I7	Native	OUT	DDPC_CTRLCLK	DisplayPort Front Panel Lower Port DDC_CLK
I8	Native	I/O	DDPC_CTRLDTA	DisplayPort Front Panel Lower Port DDC_DATA
I9	Native	OUT	DDPD_CTRLCLK	DisplayPort P-HSE2 Port DDC_CLK
I10	Native	I/O	DDPD_CTRLDTA	DisplayPort P-HSE2 Port DDC_DATA
Deep Sleep Well Group (GDP)				

GPIO Usage CM238 PCH				
GPIO	USAGE	DIR	Function	Description
0	Native	IN	BATLOW#	Not used on SC5 (pulled via resistor to +3.3V)
1	Native	IN	ACPRESENT	Not used on SC5 (pulled via resistor to +3.3V)
2	Native	IN	LAN_WAKE#	Connected to Ethernet Controller NC1 LAN_WAKE#
3	Native	IN	PWRBTN#	Power Button Event, connected to PLD
4	Native	OUT	SLP_S3#	Power Management Signal, connected to PLD
5	Native	OUT	SLP_S4#	Power Management Signal, connected to PLD
6	GPIO	IN	N/A	Not connected on SC5
7	GPIO	OUT	N/A	Not connected on SC5
8	Native	OUT	SUSCLK	Buffer Clock from RTC, connected to a Test Point
9	Native	OUT	SLP_WLAN#	Not connected on SC5
10	Native	OUT	SLP_S5#	Power Management Signal, connected to PLD
11	Native	OUT	ENABLE_NC1	Enable Ethernet Controller NC1

All GPIO groups are sourced by +3.3V supply active in power states S0-S5.

Configuration Jumpers

Loading UEFI/BIOS Setup Defaults/IEEE 1588 Pulse per Second (J-GP)

The jumper J-GP may be used to reset the UEFI/BIOS configuration settings to a default state. The UEFI/BIOS on SC5-FESTIVAL stores most of its settings in an area within the UEFI/BIOS flash, e.g. the actual boot devices. Using the jumper J-GP is only necessary, if it is not possible to enter the setup of the UEFI/BIOS. To reset the settings mount a jumper on J-GP and perform a system reset. As long as the jumper is stuffed the UEFI/BIOS will use the default configuration values after any system reset. To get normal operation again, the jumper has to be removed.

There is also an alternate function available on J-GP. Pin 1 of this jumper carries a Pulse per Second (PPS) signal according the IEEE 1588 specification when enabled by UEFI/BIOS settings. A wire may be connected to trigger events on external devices.

NOTE: The PPS signal can be gripped at the CompactPCI® Serial connector P1 pin J3 (SATA-SCL) also.

J-GP

J-GP	Function
Jumper Removed [1)]	Normal operation
Jumper Installed	UEFI/BIOS configuration reset performed

[1)] This setting is the factory default

Manufacturer Mode Jumper (J-MFG)

The jumper J-MFG is used to bring the board into the manufacturer mode. This is necessary only on board production time and should not used by customers. For normal operation the jumper should be removed. The pin header J-MFG is not stuffed on the SC5-FESTIVAL by default.

J-MFG

J-MFG	Function
Jumper Removed [1)]	Normal operation
Jumper Installed	Entering Manufacturer Mode

[1)] This setting is the factory default

RTC Reset (J-RTC)

The jumper J-RTC may be used to reset certain register bits of the battery backed RTC core within the PCH CM238. This can be necessary under rare conditions (e.g. battery undervoltage), if the CPU fails to enter the UEFI/BIOS POST after power on. Note that installing of jumper J-RTC will neither set UEFI/BIOS Setup to EKF Factory Defaults nor resets the time and date register values of the RTC (Real Time Clock). To reset the RTC core the board must be removed from the system rack. Short-circuit the pins of J-RTC for about 1 sec. Thereafter reinstall the board to the system and switch on the power. The pin header J-RTC is not stuffed on the SC5-FESTIVAL by default.

NOTE:
It is important to accomplish the RTC reset while the board has no power.

J-RTC

J-RTC	Function
Jumper Removed [1)]	Normal operation
Jumper Installed	RTC reset performed

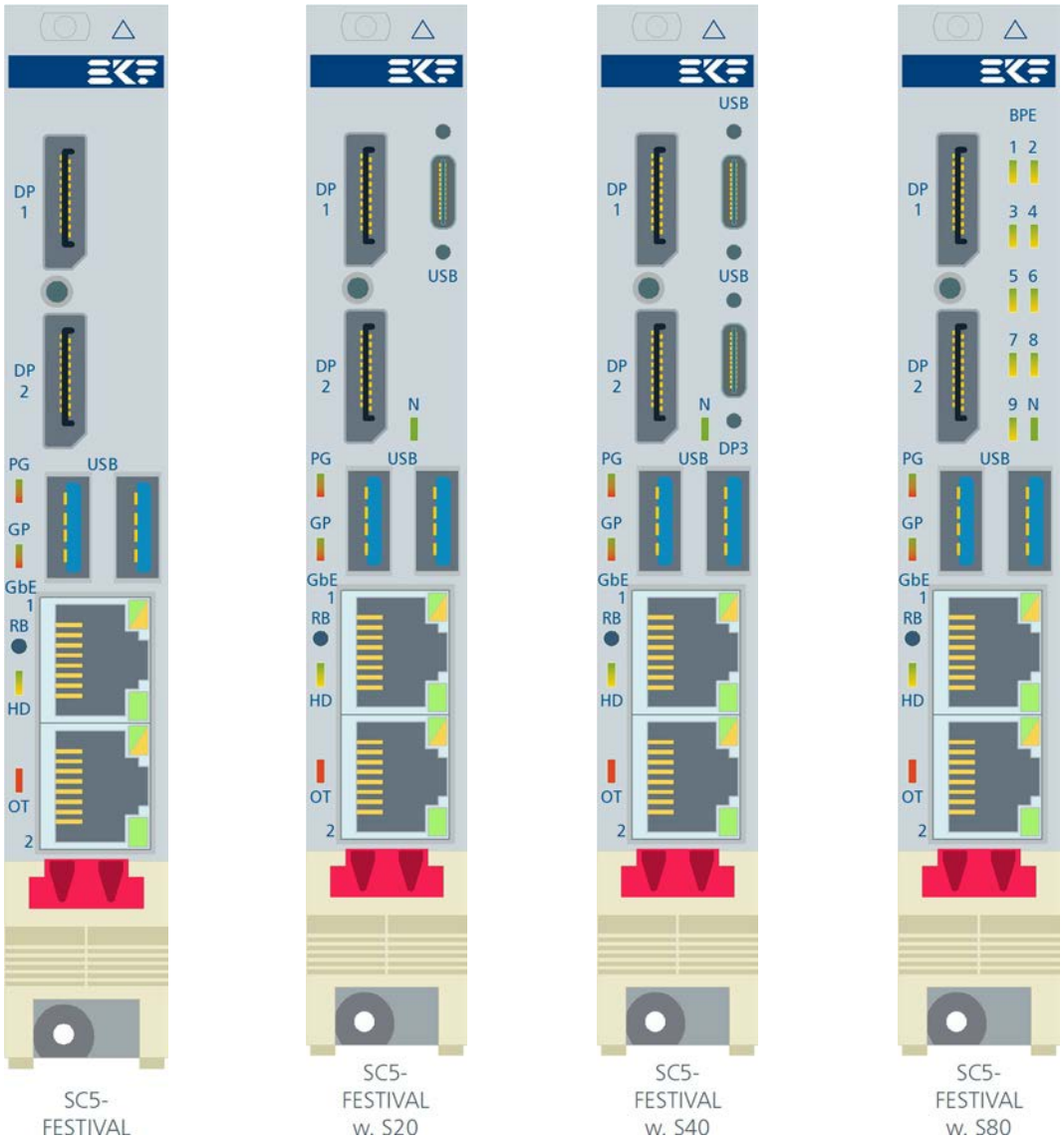
[1)] This setting is the factory default.

Connectors

Caution

Some of the internal connectors provide operating voltage (3.3V, 5V and 12V) to devices inside the system chassis, such as internal peripherals. Not all of these connectors are short circuit protected. Do not use these internal connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

Front Panel Connectors



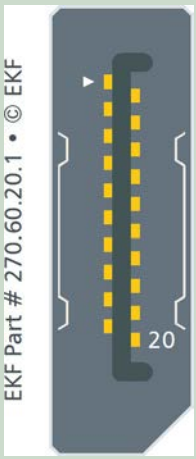
The basic SC5-FESTIVAL front panel connectors are illustrated on the left side above . If low profile mezzanine modules are employed, one or two Type-C receptacles may be available for front I/O in addition (illustrated on the right side above). Documentation on the Type-C connectors is not provided in this manual - please refer to the particular mezzanine module in use.

For 8HP/12HP front panel width assemblies together with a side card e.g. SCZ-NVM please refer to the particular side card documentation.

DisplayPort Connectors

The Intel graphics processing unit (GPU) on the SC5-FESTIVAL processor carrier card incorporates up to three external DisplayPort video channels. Two video outputs are available via the CPU card front panel (standard DisplayPort receptacles, reverse mount). A third DP signal channel is passed across the HSE2 mezzanine connector for optional use on a mezzanine card.

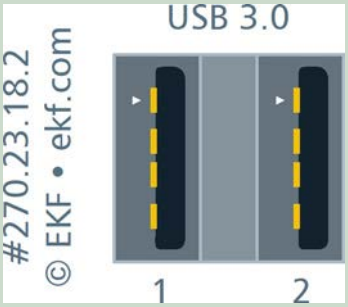
Independent operation of multiple displays (e.g. Windows® Expanded Desktop) is enabled by the Intel graphics drivers.

DP1 & DP2 • DisplayPort Video Standard DisplayPort Receptacles (Reverse Mount Type) 20-lead (270.60.20.1)				
	1	LANE0(P)	2	GND
	3	LANE0(N)	4	LANE1(P)
	5	GND	6	LANE1(N)
	7	LANE2(P)	8	GND
	9	LANE2(N)	10	LANE3(P)
	11	GND	12	LANE3(N)
	13	CONFIG1	14	CONFIG2 (GND)
	15	AUX(P)	16	GND
	17	AUX(N)	18	Hot Plug Detect
	19	Power Return	20	Power +3.3V 0.5A [1)]

[1)] Sourced via electronic power switch (back driving protected), maximum current for short circuit detection 1.5A. Voltage supply active only in power state S0.

USB Connectors

The Intel® CM238 Platform Controller Hub incorporates a four-port USB 3.0 xHCI host controller. Two ports are directly available on the SC5-FESTIVAL front panel (type A receptacle), for attachment of external USB devices.

P-USB • Dual USB 3.0 Receptacle USB 3.0 dual type A receptacle, stacked, 18-position		
	1	VBUS +5V, 1.5A max [1]
	2	USB D-
	3	USB D+
	4	GND
	5	SS RX-
	6	SS RX+
	7	GND
	8	SS TX-
	9	SS TX+

[1] +5V via 1.5A current-limited electronic power switch. The voltage is active in power states S0-S5 and may be switched off by software independently for each port.

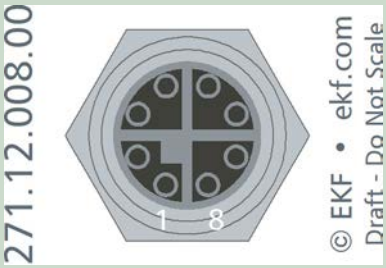
Ethernet Connectors

Gigabit Ethernet Ports 1/2 (P-ETH, RJ-45)			
	Port 1	1	NC1_MDX0+
		2	NC1_MDX0-
		3	NC1_MDX1+
		4	NC1_MDX2+
		5	NC1_MDX2-
		6	NC1_MDX1-
		7	NC1_MDX3+
		8	NC1_MDX3-
	Port 2	1	NC2_MDX0+
		2	NC2_MDX0-
		3	NC2_MDX1+
		4	NC2_MDX2+
		5	NC2_MDX2-
		6	NC2_MDX1-
		7	NC2_MDX3+
		8	NC2_MDX3-

The lower green LED indicates LINK established when continuously on, and data transfer (activity) when blinking. If the lower green LED is permanently off, no LINK is established. The upper green/yellow dual-LED signals the link speed 1Gbit/s when lit yellow, 100Mbit/s when lit green, and 10Mbit/s when off.

Option M12 X-Coded Ethernet Receptacles

As an ordering option, the RJ45 jacks can be replaced by M12 X-coded receptacles. A small mezzanine module (P01-M12) is soldered to the RJ45 footprint, resulting in an 8HP front panel assembly.

M12 X-Coded Front Panel I/O Receptacles Gigabit Ethernet • 271.12.008.20 • M12-X Flush-type socket			
	Ports 1-2	1	MDX0+
		2	MDX0-
		3	MDX1+
		4	MDX1-
		5	MDX3+
		6	MDX3-
		7	MDX2-
		8	MDX2+

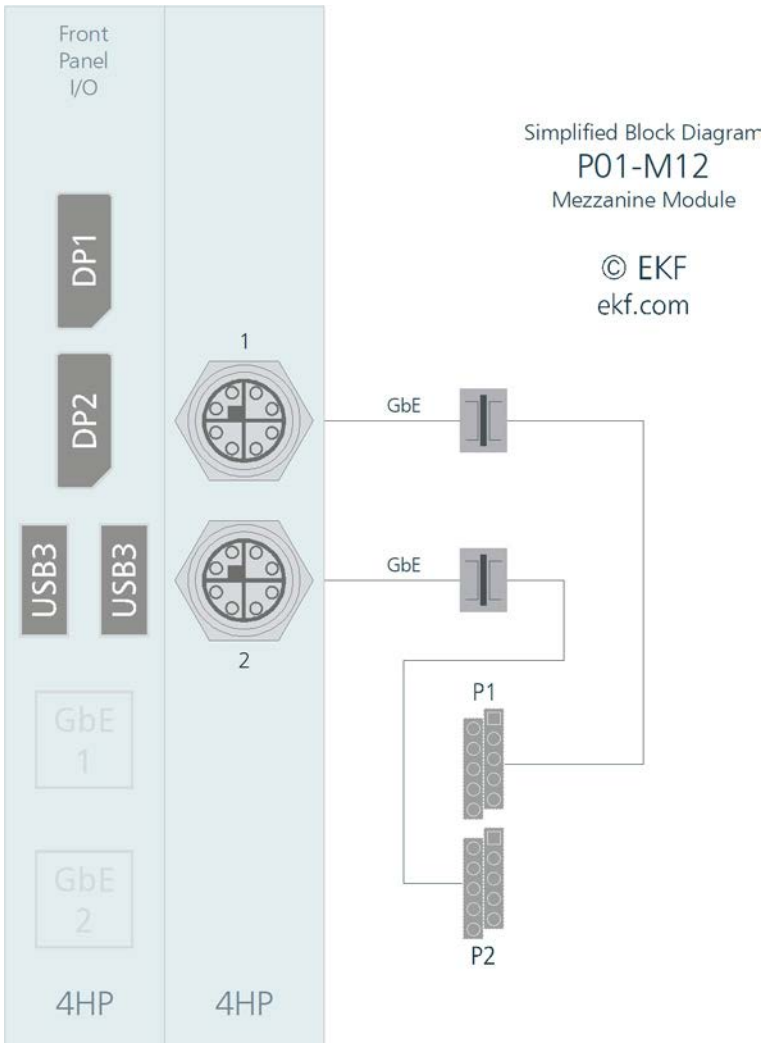
The pin numbers of an M12 X-coded connector do not reflect the RJ45 Gigabit Ethernet signal assignment. For cross-over patch cables M12 to RJ45 please refer to the table below.

M12 X	Signal Colors T568B	RJ45
1	MDX0+ white/orange	1
2	MDX0- orange	2
3	MDX1+ white/green	3
4	MDX1- green	6
5	MDX3+ white/brown	7
6	MDX3- brown	8
7	MDX2- white/blue	5
8	MDX2+ blue	4

Suitable industrial Gigabit Ethernet M12 cable assemblies can be ordered from EKF, or directly from well-known cable and connector manufacturers e.g. Metz, Phoenix, Escha and many others.

Ordering Information Cable Assemblies
Gigabit Ethernet cable M12 to M12: #271.14.008.xx (xx=length/meter)
Gigabit Ethernet cable M12 to RJ-45: #271.15.008.xx (xx=length/meter)


HSE1
EXP
M.2
M.2
ATA
6G
PCIe x4
NVMe
2
1
2242
2242
2260
2260
2280
2280
MAGMOD 1
MAGMOD 2
P01-M12
S40-NVME © EKF
PCH
CM238
CPU
XEON® E3 v6
P5
P4
P3
P2
P1
Locking Bar
P-FPH
Top Side
Component
Assembly
SC5-FESTIVAL • CompactPCI® Serial • © EKF • ekf.com


Front
Panel
I/O
DP1
DP2
USB3
USB3
GbE
1
GbE
2
4HP
4HP
1
2
GbE
GbE
P1
P2
Simplified Block Diagram
P01-M12
Mezzanine Module
© EKF
ekf.com

Mezzanine Connectors

Three connectors are available for SC5-FESTIVAL mezzanine expansion. Two high speed signal connectors (HSE1, HSE2) and in addition a legacy I/F connector (EXP) are populated on top of the CPU board.

EKF offers low profile mezzanine modules which fit into the 4HP envelope of the CPU carrier card, with varying B2B clearance from 9.5mm to 10.8mm, and also side cards for additional 4HP mounting pitch (8HP in total assembly, 18.7mm B2B). The female connector EXP is identically populated on carrier and mezzanine and requires a suitable pin header (stacker) as contact element between carrier and mezzanine in addition. The HSE1/HSE2 connectors of carrier and mezzanine are female (CPU) and male (mezzanine) pairs, selected to match the individual B2B height requirements:

HSE1/HSE2 Mezzanine Connectors	
Mezzanine Series, B2B	Connector
CPU Carrier	8mm female ERNI Microspeed 275.90.08.068.01
C4*, B2B 9.5mm	Supplement 1mm male connector for nominal height 9mm
S2*, S4*, B2B 10.0mm	Supplement 2mm male connector for nominal height 10mm
S6*, S8*, B2B 10.8mm	Supplement 2mm male connector for nominal height 10mm
SC* side card, B2B 18.7mm	Supplement 8mm male connector for nominal height 18mm

C48-M2 • Low Profile Dual M.2 SATA SSD Mezzanine Module

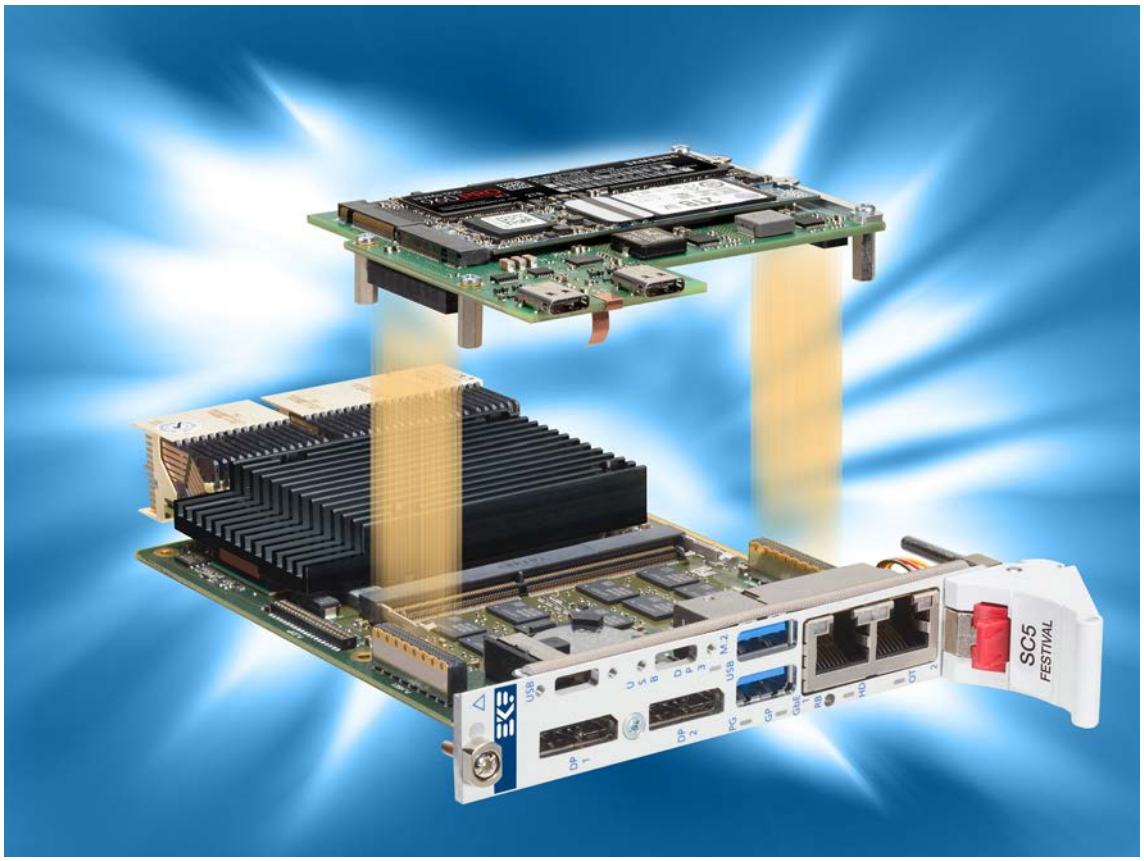
Series	Board to Board Space	HSE1	HSE2	M.2 Style	Type-C Front I/O	P6 Ethernet Backplane	Side Card Option 8HP (HSE2)
C4*	9.5mm	SATA x4 3)	1)	D3	○	○	○
S2*	10.0mm	PCIe x4, USB3	2)	D3	✓	○	✓
S4*	10.0mm	PCIe x4, USB3	PCIe x4, DP	D3	✓	○	○
S6*	10.8mm	PCIe x2, SATA x2, USB3	2)	S3	○	✓	✓
S8*	10.8mm	PCIe x4, USB3	PCIe x4, DP	S3	○	✓	○

1) HSE2 covered by mezzanine PCB - not usable for additional 8HP side card
2) HSE2 recessed on mezzanine PCB - available for additional 8HP side card (option)
3) Two SATA ports in use on mezzanine (C47: SATA 2/3, C48: SATA 1/2)

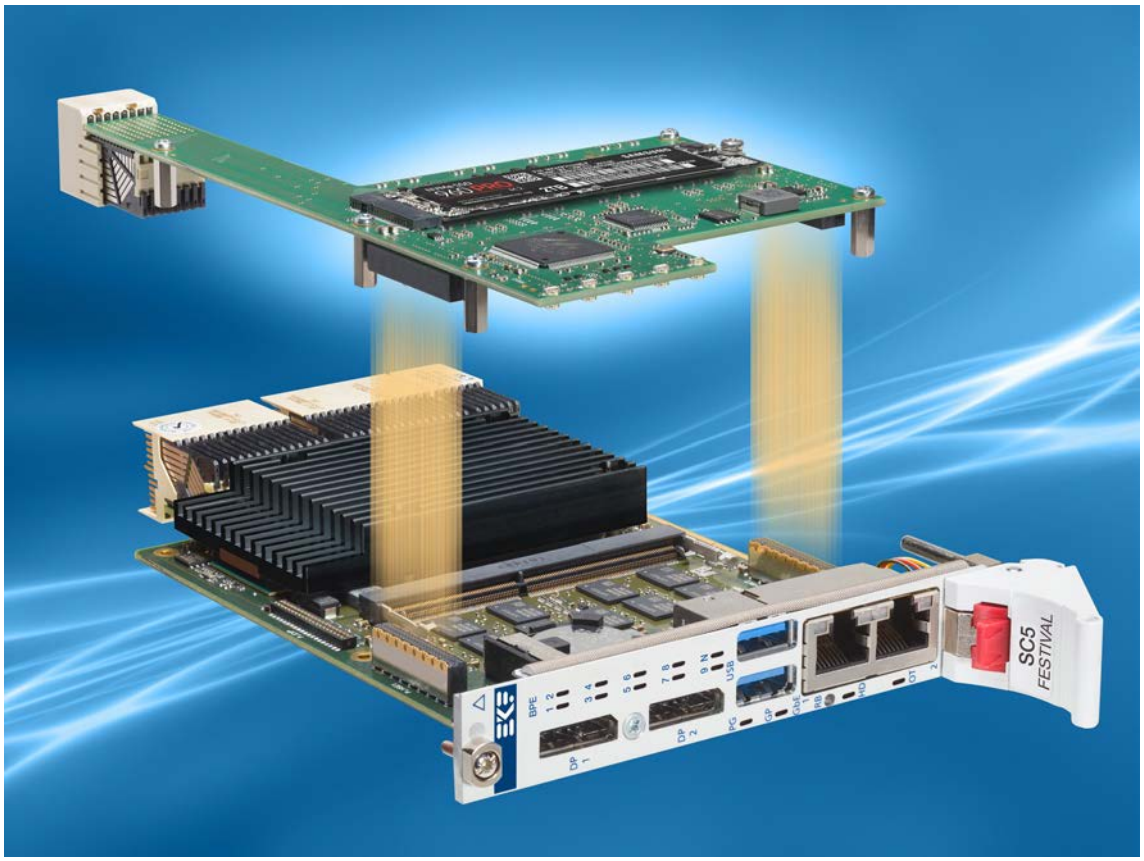
✓ Feasible (option)
○ Not scheduled or infeasible

D3 Double sided M.2 (top 1.5mm, bottom 1.35mm) or single sided M.2
S3 Single sided M.2 only (top 1.5mm)

HSE1 Connector Employed for for S2x Low Profile Mezzanines



Both HSE Connectors in Use for S4x and S8x Low Profile Mezzanines



P6 Backplane Connector w. S80-P6 Low Profile Mezzanine

8HP/12HP Assemblies w. Side Card SCZ-NVM

P-HSE1

High Speed Expansion P-HSE1			
CFG_12 [4]	a1	b1	CFG_34 [4]
1_SATA_PCIE_TXP	a2	b2	3_SATA_PCIE_TXP
1_SATA_PCIE_TXN	a3	b3	3_SATA_PCIE_TXN
GND	a4	b4	GND
1_SATA_PCIE_RXN	a5	b5	3_SATA_PCIE_RXN
1_SATA_PCIE_RXP	a6	b6	3_SATA_PCIE_RXP
GND	a7	b7	GND
2_SATA_PCIE_TXP	a8	b8	4_SATA_PCIE_TXP
2_SATA_PCIE_TXN	a9	b9	4_SATA_PCIE_TXN
GND	a10	b10	GND
2_SATA_PCIE_RXN	a11	b11	4_SATA_PCIE_RXN
2_SATA_PCIE_RXP	a12	b12	4_SATA_PCIE_RXP
GND	a13	b13	GND
1_USB2_P	a14	b14	2_USB3_TXP
1_USB2_N	a15	b15	2_USB3_TXN
GND	a16	b16	GND
2_USB2_P	a17	b17	2_USB3_RXP
2_USB2_N	a18	b18	2_USB3_RXN
GND	a19	b19	GND
1_2_USB_OC# [5]	a20	b20	PCIE_CLK_P
PLTRST#	a21	b21	PCIE_CLK_N
+3.3VS [1]	a22	b22	+5VS [1]
+3.3VS [1]	a23	b23	+5VS [1]
+3.3VA [3]	a24	b24	+5VPS [2]
+12VPS [2]	a25	b25	+12VPS [2]

[1] Power rail switched on in S0 state only
[2] Power rail switched on in S0-S4 state
[3] Power always on
[4] CFG_12/CFG_34: GND configures to SATA, OPEN or HIGH configures to PCIe
[5] Signal is 3.3V tolerant only

P-HSE2

High Speed Expansion P-HSE2				
	1_PCIE_TXP	a1	b1	3_PCIE_TXP
	1_PCIE_TXN	a2	b2	3_PCIE_TXN
	GND	a3	b3	GND
	1_PCIE_RXN	a4	b4	3_PCIE_RXN
	1_PCIE_RXP	a5	b5	3_PCIE_RXP
	GND	a6	b6	GND
	2_PCIE_TXP	a7	b7	4_PCIE_TXP
	2_PCIE_TXN	a8	b8	4_PCIE_TXN
	GND	a9	b9	GND
	2_PCIE_RXN	a10	b10	4_PCIE_RXN
	2_PCIE_RXP	a11	b11	4_PCIE_RXP
	GND	a12	b12	GND
	DP_LANE0_P	a13	b13	DP_LANE2_P
	DP_LANE0_N	a14	b14	DP_LANE2_N
	GND	a15	b15	GND
	DP_LANE1_P	a16	b16	DP_LANE3_P
	DP_LANE1_N	a17	b17	DP_LANE3_N
	GND	a18	b18	GND
	PCIE_CLK_P	a19	b19	DP_AUX_P
	PCIE_CLK_N	a20	b20	DP_AUX_N
	GND	a21	b21	DP_CFG1
	I2C_SCL [1)]	a22	b22	DP_HPD
	I2C_SDA [1)]	a23	b23	PLTRST#
	+12VPS [2)]	a24	b24	+12VPS [2)]
	+12VPS [2)]	a25	b25	+12VPS [2)]

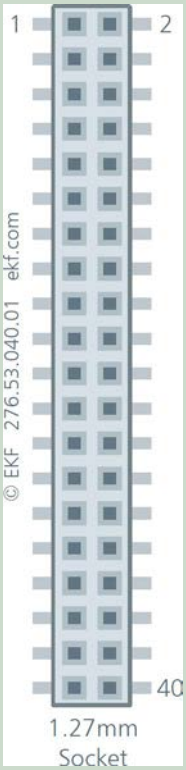
[1)] Connected to CM238 PCH I2C Bus Controller 0, 3.3V tolerant only

[2)] Power rail switched on in S0-S4 state

PCIe link width configurable via recent (2020) UEFI/BIOS & ME:
Setup (F2): Advanced -> PCI Configuration -> PCH PCI Express Configuration -> Select Link Width of PCH PCIe Controller 1-5
Available options: No override (default), 4x1, 2x2, 1x2+2x1 and 1x4

P-EXP

P-EXP • Expansion Board Interface (LPC/HD-Audio/UART) 1.27mm Socket 2 x 20 (276.53.040.01)			
GND	1	2	+3.3VS [1]
CLK_24MHZ (CLK_33MHz)	3	4	PLTRST#
LPC_AD0	5	6	LPC_AD1
LPC_AD2	7	8	LPC_AD3
LPC_FRAME#	9	10	NC (LPC_DRQ#)
GND	11	12	+3.3VS [1]
SERIRQ	13	14	PME#
SMI#	15	16	CLK_14MHZ
1_UART_TXD (FWH_ID0)	17	18	1_UART_RXD (FWH_INIT#)
RCIN# [4] (KBD_RST#)	19	20	1_UART_RTS# (A20GATE)
GND	21	22	+5VS [1]
0_UART_TXD (2_USB2_N)	23	24	0_UART_RTS# (1_USB2_N)
0_UART_RXD (2_USB2_P)	25	26	0_UART_CTS# (1_USB2_P)
1_UART_CTS# (2_USB_OC#)	27	28	XDP_RESET# [5]
I2C_SCL [3]	29	30	I2C_SDA [3]
GND	31	32	+5VS [1]
HDA_SDOUT	33	34	HDA_SDIN0
HDA_RST#	35	36	HDA_SYNC
HDA_BITCLK	37	38	HDA_SDIN1
SPEAKER	39	40	+12VPS [2]



pin orientation shows CPU carrier board top view

[1] Power rail switched on in S0 state only
[2] Power rail switched on in S0-S4 state
[3] Connected to CM238 PCH I^2C Bus Controller 0
[4] Connected to CM238 PCH pin RCIN#/GPP_A0
[5] Connected to debug port reset logic in order to force hardware reset
[6] Signals are 3.3V tolerant only

The UART pins of the P-EXP connector allow dual use - either serial I/F (native usage), or GPIO for custom specific application:
Alternate 1: 1 x UART, 4 x GPIO
Alternate 2: 8 x GPIO

Pin Headers & Debug

Front Panel Handle Microswitch Header P-FPH

The jumper P-FPH is used for attachment of an external SPDT switch. By default, P-FPH is connected across a short cable harness to a microswitch, which is integrated into the SC5-FESTIVAL front panel handle (ejector lever). The switch performs a power button event (e.g. system shutdown) by short-circuiting the pins 1 and 3 of P-FPH when activated (hold unlock button of front panel handle depressed momentarily).

P-FPH		
		
1	black	Microswitch Pole (Common), Wired to PLD
2	red	Microswitch Throw - F/P Handle Locked Position, NC
3	yellow	Microswitch Throw - F/P Handle Unlocked Position, Wired to GND

PLD Programming Header P-ISP

The SC5-FESTIVAL is provided with a powerful PLD (in-System Programmable Logic Device) which replaces legacy glue logic. The programming header P-ISP is not stuffed (in use for manufacturing only). Its footprint is situated at the bottom side of the board.

P-ISP

1	+3.3V
2	TDO
3	TDI
4	NC
5	KEY
6	TMS
7	GND
8	TCK

Processor Debug Header P-XDP

The SC5-FESTIVAL may be equipped with a 60-position processor debug header for hard- and software debugging (specified by Intel® as XDP-60 Pin Platform Connection). The connector is suitable for installation of a flat cable, in order to attach an JTAG debugger (emulator) such as the Intel® ITP-XDP3.

The header P-XDP would be mounted on the PCB bottom side. Since its heights is with 5mm much higher than the allowed 2.1mm it is not stuffed by default.

P-XDP Processor Debug Connector			
1	XDP_Pin#1	GND	2
3	OBSFN_A0	OBSFN_C0	4
5	OBSFN_A1	OBSFN_C1	6
7	GND	GND	8
9	OBSDATA_A0	OBSDATA_C0	10
11	OBSDATA_A1	OBSDATA_C1	12
13	GND	GND	14
15	OBSDATA_A2	OBSDATA_C2	16
17	OBSDATA_A3	OBSDATA_C3	18
19	GND	GND	20
21	OBSFN_B0	OBSFN_D0	22
23	OBSFN_B1	OBSFN_D1	24
25	GND	GND	26
27	OBSDATA_B0	OBSDATA_D0	28
29	OBSDATA_B1	OBSDATA_D1	30
31	GND	GND	32
33	OBSDATA_B2	OBSDATA_D2	34
35	OBSDATA_B3	OBSDATA_D3	36
37	GND	GND	38
39	HOOK0	HOOK4	40
41	HOOK1	HOOK5	42
43	VCCOBS_AB	VCCOBS_CD	44
45	HOOK2	HOOK6	46
47	HOOK3	HOOK7	48
49	GND	GND	50
51	XDP_SDA	XDP_TDO	52
53	XDP_SCL	XDP_TRST#	54
55	XDP_TCK1	XDP_TDI	56
57	XDP_TCK0	XDP_TMS	58
59	GND	XDP_PRESENT#	60

CompactPCI® Serial Backplane Connectors P1 - P6

The SC5-FESTIVAL is provided with five high speed backplane connectors P1 - P5, compliant with the CompactPCI® Serial specification (pin mapping for system boards).

The PCI Express® Lanes 1_PE_* to 2_PE_* are derived directly from the processor and capable to transfer 8GT/s (PCIe Gen3). These lanes are assigned via the backplane to the CompactPCI® Serial fat pipe slots, for a maximum link width of 8 each.

P1 CompactPCI® Serial Slot Backplane Connector Type A
EKF Part #250.3.1206.20.02 • 72 pos. 12x6, 14mm Width

P1	A	B	C	D	E	F	G	H	I	J	K	L
6	GND	1 PE TX02+ 1)	1 PE TX02- 1)	GND	1 PE RX02+ 1)	1 PE RX02- 1)	GND	1 PE TX03+ 1)	1 PE TX03- 1)	GND	1 PE RX03+	1 PE RX03-
5	1 PE TX00+	1 PE TX00-	GND	1 PE RX00+	1 PE RX00-	GND	1 PE TX01+	1 PE TX01-	GND	1 PE RX01+	1 PE RX01-	GND
4	GND	1 USB2+	1 USB2-	GND	RSV	RSV	GND	1 SATA TX+	1 SATA TX-	GND	1 SATA RX+	1 SATA RX-
3	1 USB3 TX+	1 USB3 TX-	PWR BTN#	1 USB3 RX+	1 USB3 RX-	PWR_ FAIL#	SATA SDI 4) 5)	SATA SDO 3) 4)	GA2	SATA SCL 2) 4)	SATA SL 4)	GA3
2	GND	I2C SCL	I2C SDA	GND	PS_ ON#	RST#	GND	PRST#	WAKE_ IN#	GND	RSV	SYS EN#
1	+12V	+5V STBY	GND	+12V	+12V	GND	+12V	+12V	GND	+12V	+12V	GND

pin positions printed gray: not connected

1) Polarity inversion was made on these lanes on SC5-FESTIVAL for better routing. This is allowed according the "PCI Express Base Specification 3.0" and has no effect on function or performance of the link. The pin-out shown is as per specification.
2) This pin may carry the IEEE 1588 Pulse per Second (PPS) signal when enabled within UEFI/BIOS settings.
3) This pin may carry the IEEE 1588 Pulse per Minute (PPM) signal when enabled within UEFI/BIOS settings.
4) 10kΩ Pull-Up resistor to +3.3V when board is inserted in system controller slot.
5) This pin is connected to the CM238 PCH GPIO GPP_F12

P2 CompactPCI® Serial Slot Backplane Connector Type B EKF Part #250.3.1208.20.00 • 96 pos. 12x8, 16mm Width												
P2	A	B	C	D	E	F	G	H	I	J	K	L
8	GND	IO	IO	GND	2 USB2+	2 USB2-	GND	3 USB2+	3 USB2-	GND	4 USB2+	4 USB2-
7	IO	IO	GND	IO	IO	GND	IO	IO	GND	IO	IO	GND
6	GND	2 PE TX06+ 1)	2 PE TX06- 1)	GND	2 PE RX06+	2 PE RX06-	GND	2 PE TX07+	2 PE TX07-	GND	2 PE RX07+	2 PE RX03-
5	2 PE TX04+ 1)	2 PE TX04- 1)	GND	2 PE RX04+	2 PE RX04-	GND	2 PE TX05+	2 PE TX05-	GND	2 PE RX05+	2 PE RX05-	GND
4	GND	2 PE TX02+ 1)	2 PE TX02- 1)	GND	2 PE RX02+	2 PE RX02-	GND	2 PE TX03+	2 PE TX03-	GND	2 PE RX03+	2 PE RX03-
3	2 PE TX00+ 1)	2 PE TX00- 1)	GND	2 PE RX00+	2 PE RX00-	GND	2 PE TX01+	2 PE TX01-	GND	2 PE RX01+	2 PE RX01-	GND
2	GND	1 PE TX06+ 1)	1 PE TX06- 1)	GND	1 PE RX06+ 1)	1 PE RX06- 1)	GND	1 PE TX07+ 1)	1 PE TX07- 1)	GND	1 PE RX07+	1 PE RX07-
1	1 PE TX04+ 1)	1 PE TX04- 1)	GND	1 PE RX04+ 1)	1 PE RX04- 1)	GND	1 PE TX05+	1 PE TX05-	GND	1 PE RX05+	1 PE RX05-	GND

pin positions printed gray: not connected

1) Polarity inversion was made on these lanes on SC5-FESTIVAL for better routing. This is allowed according the "PCI Express Base Specification 3.0" and has no effect on function or performance of the link. The pin-out shown is as per specification.

P3 CompactPCI® Serial Slot Backplane Connector Type B EKF Part #250.3.1208.20.00 • 96 pos. 12x8, 16mm Width												
P3	A	B	C	D	E	F	G	H	I	J	K	L
8	GND	7 SATA TX+ 1)	7 SATA TX- 1)	GND	7 SATA RX+ 1)	7 SATA RX- 1)	GND	8 SATA TX+ 1)	8 SATA TX- 1)	GND	8 SATA RX+ 1)	8 SATA RX- 1)
7	5 SATA TX+ 2)	5 SATA TX- 2)	GND	5 SATA RX+ 2)	5 SATA RX- 2)	GND	6 SATA TX+ 2)	6 SATA TX- 2)	GND	6 SATA RX+ 2)	6 SATA RX- 2)	GND
6	GND	3 SATA TX+ 2)	3 SATA TX- 2)	GND	3 SATA RX+ 2)	3 SATA RX- 2)	GND	4 SATA TX+ 2)	4 SATA TX- 2)	GND	4 SATA RX+ 2)	4 SATA RX- 2)
5	8 USB3 TX+	8 USB3 TX-	GND	8 USB3 RX+	8 USB3 RX-	GND	2 SATA TX+	2 SATA TX-	GND	2 SATA RX+	2 SATA RX-	GND
4	GND	6 USB3 TX+	6 USB3 TX-	GND	6 USB3 RX+	6 USB3 RX-	GND	7 USB3 TX+	7 USB3 TX-	GND	7 USB3 RX+	7 USB3 RX-
3	4 USB3 TX+	4 USB3 TX-	GND	4 USB3 RX+	4 USB3 RX-	GND	5 USB3 TX+	5 USB3 TX-	GND	5 USB3 RX+	5 USB3 RX-	GND
2	GND	2 USB3 TX+	2 USB3 TX-	GND	2 USB3 RX+	2 USB3 RX-	GND	3 USB3 TX+	3 USB3 TX-	GND	3 USB3 RX+	3 USB3 RX-
1	5 USB2+	5 USB2-	GND	6 USB2+	6 USB2-	GND	7 USB2+	7 USB2-	GND	8 USB2+	8 USB2-	GND

pin positions printed gray: not connected

1) This SATA channel is derived from the PCH CM238, capable of up to 6Gbps.
2) This SATA channel is derived from the 88SE9230 SATA 6G host controller.

P4 CompactPCI® Serial Slot Backplane Connector Type B EKF Part #250.3.1208.20.00 • 96 pos. 12x8, 16mm Width												
P4	A	B	C	D	E	F	G	H	I	J	K	L
8	GND	6 PE TX02+	6 PE TX02-	GND	6 PE RX02+	6 PE RX02-	GND	6 PE TX03+	6 PE TX03-	GND	6 PE RX03+	6 PE RX03-
7	6 PE TX00+	6 PE TX00-	GND	6 PE RX00+	6 PE RX00-	GND	6 PE TX01+	6 PE TX01-	GND	6 PE RX01+	6 PE RX01-	GND
6	GND	5 PE TX02+	5 PE TX02-	GND	5 PE RX02+	5 PE RX02-	GND	5 PE TX03+	5 PE TX03-	GND	5 PE RX03+	5 PE RX03-
5	5 PE TX00+	5 PE TX00-	GND	5 PE RX00+	5 PE RX00-	GND	5 PE TX01+	5 PE TX01-	GND	5 PE RX01+	5 PE RX01-	GND
4	GND	4 PE TX02+	4 PE TX02-	GND	4 PE RX02+	4 PE RX02-	GND	4 PE TX03+	4 PE TX03-	GND	4 PE RX03+	4 PE RX03-
3	4 PE TX00+	4 PE TX00-	GND	4 PE RX00+	4 PE RX00-	GND	4 PE TX01+	4 PE TX01-	GND	4 PE RX01+	4 PE RX01-	GND
2	GND	3 PE TX02+	3 PE TX02-	GND	3 PE RX02+	3 PE RX02-	GND	3 PE TX03+	3 PE TX03-	GND	3 PE RX03+	3 PE RX03-
1	3 PE TX00+	3 PE TX00-	GND	3 PE RX00+	3 PE RX00-	GND	3 PE TX01+	3 PE TX01-	GND	3 PE RX01+	3 PE RX01-	GND

pin positions printed gray: not connected

P5 CompactPCI® Serial Slot Backplane Connector Type C EKF Part #250.3.1206.20.00 • 72 pos. 12x6, 12mm Width												
P5	A	B	C	D	E	F	G	H	I	J	K	L
6	5 PE CLKE#	5 PE CLK+	5 PE CLK-	6 PE CLKE#	6 PE CLK+	6 PE CLK-	7 PE CLKE#	7 PE CLK+	7 PE CLK-	8 PE CLKE#	8 PE CLK+	8 PE CLK-
5	1 PE CLK+	1 PE CLK-	1 PE CLKE#	2 PE CLK+	2 PE CLK-	2 PE CLKE#	3 PE CLK+	3 PE CLK-	3 PE CLKE#	4 PE CLK+	4 PE CLK-	4 PE CLKE#
4	GND	8 PE TX02+	8 PE TX02-	GND	8 PE RX02+	8 PE RX02-	GND	8 PE TX03+	8 PE TX03-	GND	8 PE RX03+	8 PE RX03-
3	8 PE TX00+	8 PE TX00-	GND	8 PE RX00+ 1)	8 PE RX00- 1)	GND	8 PE TX01+	8 PE TX01-	GND	8 PE RX01+	8 PE RX01-	GND
2	GND	7 PE TX02+	7 PE TX02-	GND	7 PE RX02+	7 PE RX02-	GND	7 PE TX03+	7 PE TX03-	GND	7 PE RX03+	7 PE RX03-
1	7 PE TX00+	7 PE TX00-	GND	7 PE RX00+	7 PE RX00-	GND	7 PE TX01+	7 PE TX01-	GND	7 PE RX01+	7 PE RX01-	GND

pin positions printed gray: not connected

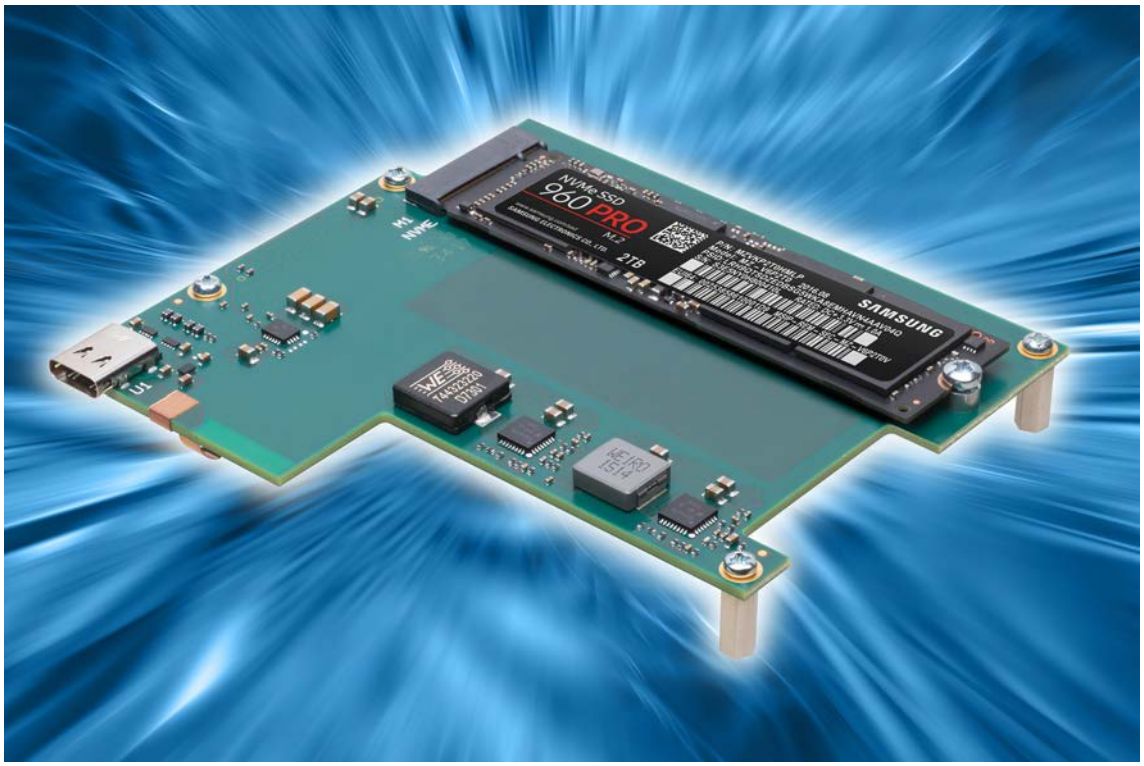
1) Polarity inversion was made on these lanes on SC5-FESTIVAL for better routing. This is allowed according the "PCI Express Base Specification 3.0" and has no effect on function or performance of the link. The pin-out shown is as per specification.

P6 CompactPCI® Serial Slot Backplane Connector Type D EKF Part #250.3.1208.20.02 • 96 pos. 12x8, 18mm width												
P6	A	B	C	D	E	F	G	H	I	J	K	L
8	GND	8 ETH A+	8 ETH A-	GND	8 ETH B+	8 ETH B-	GND	8 ETH C+	8 ETH C-	GND	8 ETH D+	8 ETH D-
7	7 ETH A+	7 ETH A-	GND	7 ETH B+	7 ETH B-	GND	7 ETH C+	7 ETH C-	GND	7 ETH D+	7 ETH D-	GND
6	GND	6 ETH A+	6 ETH A-	GND	6 ETH B+	6 ETH B-	GND	6 ETH C+	6 ETH C-	GND	6 ETH D+	6 ETH D-
5	5 ETH A+	5 ETH A-	GND	5 ETH B+	5 ETH B-	GND	5 ETH C+	5 ETH C-	GND	5 ETH D+	5 ETH D-	GND
4	GND	4 ETH A+	4 ETH A-	GND	4 ETH B+	4 ETH B-	GND	4 ETH C+	4 ETH C-	GND	4 ETH D+	4 ETH D-
3	3 ETH A+	3 ETH A-	GND	3 ETH B+	3 ETH B-	GND	3 ETH C+	3 ETH C-	GND	3 ETH D+	3 ETH D-	GND
2	GND	2 ETH A+	2 ETH A-	GND	2 ETH B+	2 ETH B-	GND	2 ETH C+	2 ETH C-	GND	2 ETH D+	2 ETH D-
1	1 ETH A+	1 ETH A-	GND	1 ETH B+	1 ETH B-	GND	1 ETH C+	1 ETH C-	GND	1 ETH D+	1 ETH D-	GND

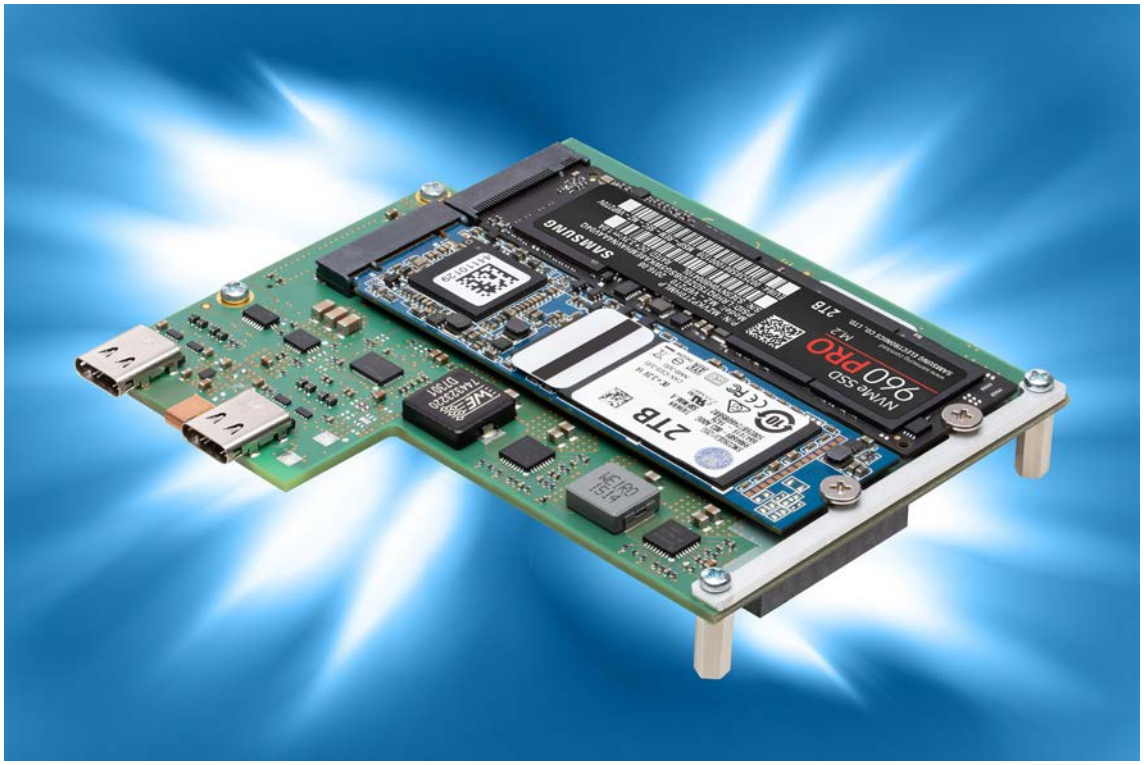
pin positions printed gray: not connected

Please note:

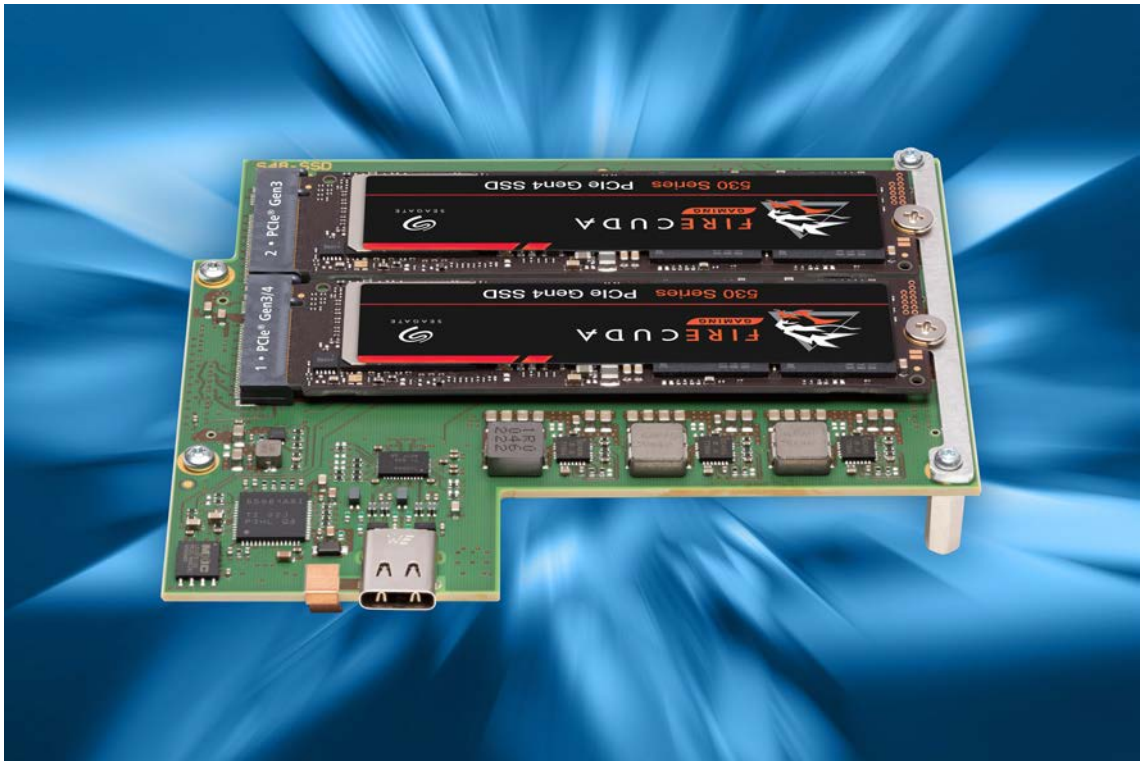
The backplane connector P6 is intentionally not populated on the SC5-FESTIVAL CPU carrier card itself, since many projects do not require a network enabled backplane configuration. Instead, P6 is provided on a low profile mezzanine module (S80-P6), which fits on the mezzanine connectors HSE1 and HSE2. On the S80-P6, all GbE ports P6(1-8) are wired across magnetics modules to a GbE switch (Marvell Peridot), which is internally connected to a PCI Express® GbE controller (I210-IS). For details please refer to the S80-P6 documentation.



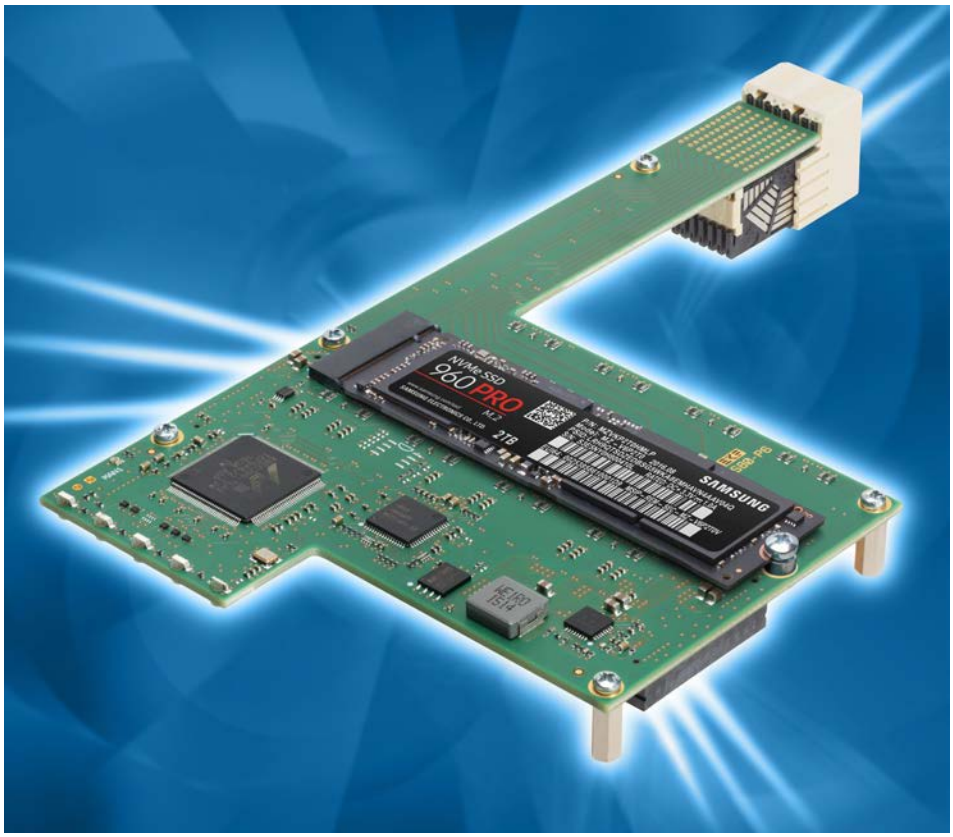
S20-NVME Mezzanine Module



S40-NVME Mezzanine Modul



S48-SSD • Dual M.2 NVMe Mass Storage



S80-P6 Mezzanine Module

SC5-FESTIVAL w. S80-P6

8HP/12HP Assemblies w. Side Card

Related Information	
SC5-FESTIVAL Home	https://www.ekf.com/s/sc5/sc5.html
SC5-FESTIVAL User Guide	https://www.ekf.com/s/sc5/sc5_ug.pdf
S20-NVME Low Profile Mezzanine	https://www.ekf.com/s/s20/s20.html
S40-NVME Low Profile Mezzanine	https://www.ekf.com/s/s40/s40.html
S42-MC Low Profile Mezzanine	https://www.ekf.com/s/s42/s42.html
S48-SSD Low Profile Mezzanine	https://www.ekf.com/s/s48/s48.html
S80-P6 Low Profile Mezzanine	https://www.ekf.com/s/s80/s80.html
S82-P6 Low Profile Mezzanine	https://www.ekf.com/s/s82/s82.html
S83-P6 Low Profile Mezzanine	https://www.ekf.com/s/s83/s83.html
SCJ-VEENA Mezzanine Side Card	https://www.ekf.com/s/scj/scj.html
SCL-RHYTHM Mezzanine Side Card	https://www.ekf.com/s/scl/scl.html
SCX-PCIE Mezzanine Side Card	https://www.ekf.com/s/scx/scx.html
SCZ-NVM Mezzanine Side Card	https://www.ekf.com/s/scz/scz.html
ECX-PCIE Mezzanine Side Card	https://www.ekf.com/e/ecx/ecx.html
PCU-P400-UPTEMPO	https://www.ekf.com/p/pcu/pcu.html
Mezzanine Connectors Explained	https://www.ekf.com/s/mezzanine_connectors.pdf

General Information CompactPCI® Serial	
CompactPCI® Serial Concise Overview	https://www.ekf.com/s/serial_concise.pdf
CompactPCI® Serial All You Need to Know	https://www.ekf.com/s/smart_solution.pdf
CompactPCI® Serial Home	https://www.ekf.com/s/serial.html

Ordering Information
For popular SC5-FESTIVAL SKUs please refer to https://www.ekf.com/liste/liste_21.html#SC5
For new mezzanine connector based low profile modules please refer to https://www.ekf.com/liste/liste_21.html#S20

Mechanical Details

Beyond All Limits:

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